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A Three-Dimensional Microfabrication Technology on Highly Structured Surfaces

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This study presents a simple process to realize the lithography and deposition on a complicated three-dimensional (3D) substrate surface conformally. The 3D lithography and patterning on a highly structured surface is implemented using the self-assembled monolayer (SAM) coating and the plasma treatment. Moreover, the selective film deposition on a 3D surface and even underneath the suspended microstructures is realized using the contact displacement electroless plating. In applications, the Cu film was conformally plated and patterned on a Si substrate with 50–200 μm deep cavities and 54.7–90° sidewalls. Moreover, the Cu electrode underneath suspended microbeams was also plated.
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Planar fabrication processes such as photolithography and thin-film deposition are frequently limited to the substrate surface topology. In this regard, the microelectromechanical systems (MEMS) devices which have more complicated surface profiles are significantly influenced by this process limitation. The realization of lithography and thin-film deposition processes over highly structured three-dimensional (3D) surfaces are of crucial importance for MEMS. The planar fabrication techniques on highly structured 3D surface have been extensively investigated. For instance, the modified spin coating approach has been discussed in Ref. 1. The electrodeposition (ED) of photoresist on highly structured surfaces is investigated in Ref. 2-5. The spray-coating technique for 3D structures fabrication is reported in Ref. 6 and 7. However, the thickness uniformity of the resist at the corners of the etched cavity is still a process consideration.[8] The very expensive projection exposure system is required for the approach in Ref. 7. Moreover, the existing ED and spray technologies are still not able to coat PR on substrate with suspended MEMS structures.

This study attempts to conformally fabricate microstructures on highly structured Si surfaces and further integrate these 3D microstructures with suspended MEMS devices, as illustrated in Fig. 1. The present process contains three key steps: (*i*) the plasma treatment,[9] (*ii*) the octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) coating,[10] and (*iii*) the contact displacement electroless (CDE) plating.[11] These techniques are employed to replace the conventional photolithography and film deposition processes on highly structured 3D surfaces. According to the characteristics of SAM coatings, CDE plating, and plasma treatment, conformal film deposition and patterning on highly structured 3D surfaces is achieved.

Fabrication Processes

Figure 2 illustrates the process steps to fabricate the devices in Fig. 1. As shown in Fig. 2a, the process began with O_2 or H_2 plasma treatments on Si substrate with deep cavities and suspended structures. The plasma treatments were operated in a plasma-enhanced chemical vapor deposition (PECVD) reaction chamber for about 30 min. The O_2 and H_2 plasma conditions were 250°C/500 mTorr at 300 W power. After that, the surface of silicon including the cavity formed the Si–O or Si–H bonds, as shown in Fig. 2b. The OTS SAM coating was employed to form the pattern transfer layer. During coating, the silicon substrate was immersed into an anhydrous toluene solution containing 1 vol % OTS for 1 h under the N_2 atmosphere. Thus, the Si surface including the deep cavities was fully and conformally covered with the OTS. As shown in Fig. 2c, the OTS patterns were defined on the highly structured surface by shadow mask or by suspended structures using the collimated O_2 plasma. This O_2 plasma patterning process was operated in a high-density plasma reactive ion etching (HDP-RIE) system. The variation of pattern dimension (linewidth) from the top surface of the substrate to the bottom surface of the cavity was tuned by varying O_2 plasma conditions such as the (inductively coupled plasma) (ICP) radio frequency (rf) power and dc bias. After that, the OTS was patterned by the O_2 plasma so as to selectively expose the Si–O bond regions on the substrate, as shown in Fig. 2d1. In addition, the O_2 plasma could further replace the same Si–H bond by Si–O bond, as in Fig. 2d2. A thin Cu layer was selectively plated using the CDE plating process,[11] as in Fig. 2e. The Si–H surface in Fig. 2d had the highest CDE Cu plating rate, whereas the OTS/Si–O had the lowest CDE Cu plating rate. The mechanism will be detailed later. Thus, the Cu seed layer in Fig. 2d1 was selectively plated on the Si–O region, and the Cu seed layer in Fig. 2d2 was only plated on the Si–H region.

The CDE plating in Fig. 2e is a selective metallization process by means of selective displacement of the metal seed layer and electroless plating. In general, the noble metals, such as Pd, Au, etc., which have high standard oxidation potentials, is preferred for CDE plating. This study selected the Cu as the metal layer. In general, the contact displacement of Cu ions from silicon is carried out by the electrochemical redox between Si^0 and Cu^{2+} ions in an aqueous solution containing F^- ions[11]

$$\text{Anode} \quad Si_{(s)} + 6F^-_{(aq)} \rightarrow SiF^{2-}_{6\ (aq)} + 4e^- \quad [1]$$

$$\text{Cathode} \quad Cu^{2+}_{(aq)} + 2e^- \rightarrow Cu_{(s)} \quad [2]$$

$$\text{Overall} \quad Si_{(s)} + 6F^-_{(aq)} + 2Cu^{2+}_{(aq)} \rightarrow 2Cu_{(s)} + SiF^{2-}_{6\ (aq)} \quad [3]$$

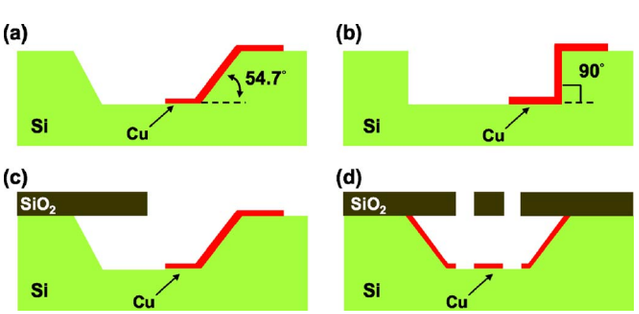

Figure 1. 3D Cu patterns processes distributed on highly structured silicon surfaces with (a) 54.7° sidewall cavities, (b) 90° sidewall cavities, (c) 54.7° sidewall cavities, with suspended structure, and (d) underneath the suspended microstructures.

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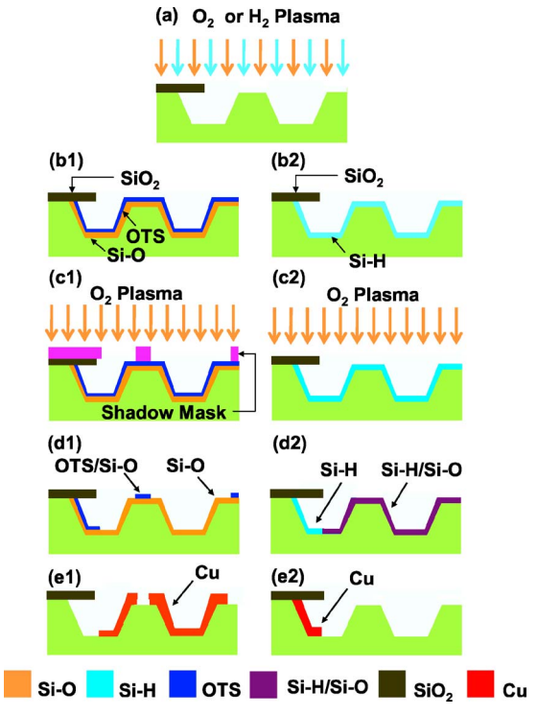

Figure 2. The 3D lithography and deposition process for fabricating microstructures on highly structured silicon surfaces and further integrating 3D microstructures with suspended MEMS devices.

Thus, the Cu seed layer was selectively plated in plating bath containing 7.5 g/L cupric sulfate ($CuSO_4$) and dilute 1% buffered oxide etch (BOE) solution (6 parts of 40% NH_4F and 1 part of 49% HF) at an ambient temperature for 30–60 s. As shown in Fig. 2d1, the BOE was used to remove the Si–O bond first, and then the BOE also provided the F^- ions for the oxidation reaction in Eq. 1. Meanwhile, the Si–O bond covered by OTS was prevented from attacking by the BOE, and the Si underneath was not replaced by Cu. As shown in Fig. 2d2, the etching rate of the Si–H bond in BOE was higher than that of the Si–H/Si–O bond. Hence, the Si under the Si–O bond was not replaced by Cu^{2+} ions. In summary, for substrate with different surfaces, the duration of replacing Si by Cu using CDE was OTS/Si–O (95 s) > Si–O (62 s) > Si–H/Si–O (34 s) > Si–H (15 s). In short, the Si atom on the substrate surface can be selectively replaced by Cu atoms after these treatments. The CDE process will not be self-terminated; it can be stopped by moving the sample from chemical solution into deionized water. In general, the thickness of the Cu layer ranges from several nanometers to several micrometers by the CDE process. The sheet resistance of the deposited Cu was measured with a four-point probe station (NAPSON RT-7), and the resistivity was extracted from the measured resistance and film thickness. In summary, the present process steps mainly consist of the plasma treatment, the OTS SAM coating, and the CDE plating. Briefly, the uncollimated plasma and SAM coating are used to perform the surface modification on highly structured Si surfaces, so as to provide the selectivity during CDE plating. In addition, the 3D lithography and patterning on the highly structured surface is implemented using the SAM coating and collimated plasma. Finally, the selective film deposition on the 3D surface and even underneath the suspended microstructures is realized using the CDE plating.

Results and Discussion

The copper film has been fabricated on various highly structured Si surfaces. In this study, the actual thickness of the Cu films was

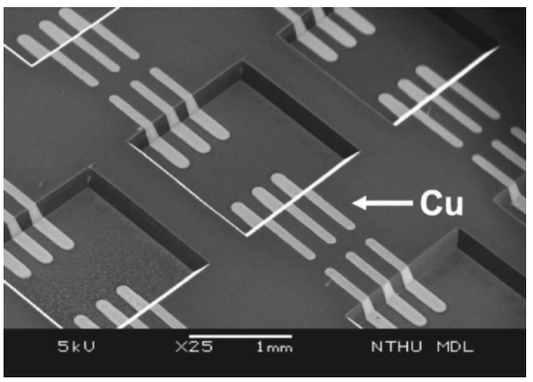

Figure 3. SEM micrographs of 3D Cu pattern arrays on silicon cavities (54.7° sidewall).

150–250 nm. The fabrication results were observed by scanning electron microscope (SEM) and characterized by X-ray diffraction (XRD). The phase and crystal structure were identified with an X-ray diffractometer with a wavelength of Cu $K\alpha_1$ (1.5406 Å).[12] The JCPDS (Joint Committee on Powder Diffraction Standards) data of copper films are no. 03-1005 and 04-0836. Figure 3 shows SEM micrographs of typical 3D Cu patterns (30–100 μm linewidth) distributed on silicon surface with 150 μm deep anisotropically etched cavities. These 3D Cu patterns were fabricated using the processes in Fig. 2b1–2e1. Figure 4 shows the XRD spectrum of a Cu film on a silicon surface prepared by the CDE plating. It shows that ⟨111⟩ is the preferred orientation for the plated copper film, and the copper with ⟨200⟩ direction is relatively weak. All the peaks obtained are well matched with the JCPDS data (File no. 03-1005 and 04-0836). In this study, the pattern defined by the plasma treatment in Fig. 2c was influenced by the collimation of the plasma. Thus, the linewidth may vary on the highly structured 3D surface. This study employed the line pattern in Fig. 3 to investigate the variation of linewidth with O_2 plasma (in Fig. 2c) of conditions. Figure 5 shows the linewidth deviation test between the top and bottom surfaces (120 μm deep) for three different ICP rf powers and dc biases of the O_2 plasma. The designed linewidth is 100 μm. The symbols W_0 and W_1 indicate the linewidth on the top and bottom surfaces, respectively, and the linewidth deviation $\Delta W = W_1 - W_0$. As the ICP rf power increases, the linewidth deviation is significantly reduced. Furthermore, as the dc bias increases, the linewidth

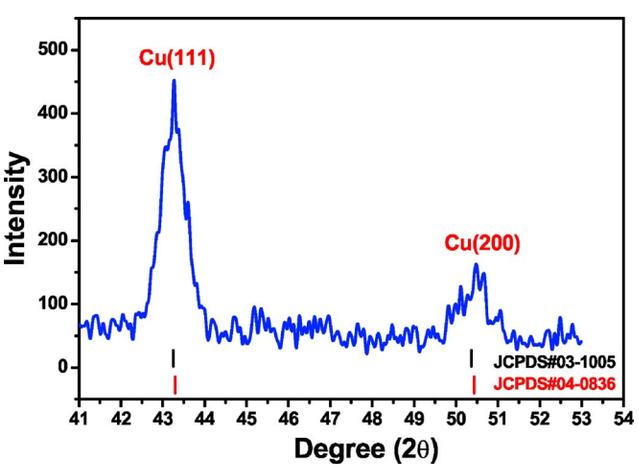

Figure 4. XRD diffraction pattern of copper film metallization on silicon cavity surfaces by the CDE plating method.

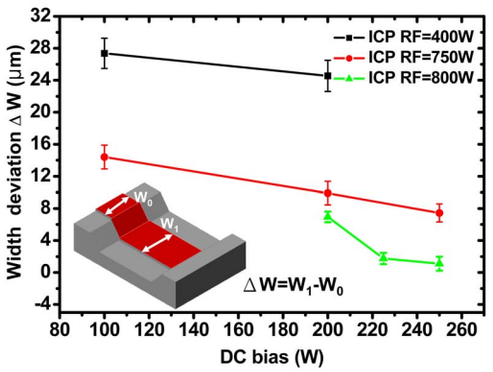

Figure 5. The linewidth deviation between the top and bottom silicon surfaces vs O_2 plasma conditions including ICP rf powers and dc biases.

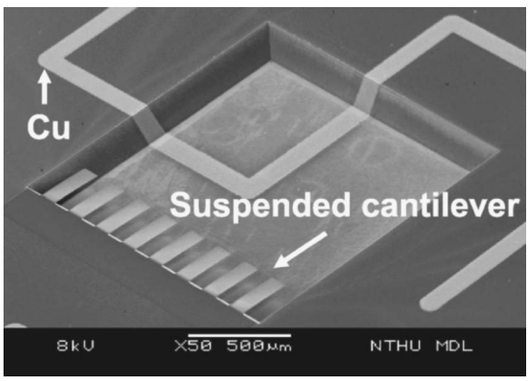

Figure 7. SEM micrographs of 3D Cu patterns distributed on highly structured silicon surfaces with 54.7° sidewall cavities with suspended structure.

deviation is also reduced. The linewidth deviation ΔW was tuned close to zero when ICP rf power and dc bias were 800 and 250 W, respectively.

The SEM micrograph in Fig. 6a shows that the Cu film was patterned and plated on a near 90° Si sidewall (50 μm deep). The inset in Fig. 6a shows the edge of the near 90° sidewall. These results demonstrate the concept illustrated in Fig. 1b. The Cu film was further plated and patterned on more complicated Si surface shown in Fig. 6b. The 3D Cu wires were distributed over the Si surface with several anisotropically etched 200 μm deep cavities. The cavities contain sidewalls of 90° (by ICP) and 54.7° (by tetramethylammonium hydroxide). It is difficult for the existing 3D patterning techniques[1-7] to conduct photolithography on Si substrate with 90° sidewalls, whether using contact or projection printing. The photoresist (2–50 μm) on the 90° sidewalls cannot be properly exposed in Ref. 1-7 because it is parallel to the incident light beam during exposure. This study employed the 5 nm OTS SAM to act as the resist, so that it was properly patterned by O_2 plasma even at the 90° sidewalls. Since the collimation of O_2 plasma was not perfectly orthogonal with the substrate surface, it is not necessary to tilt the substrate during the plasma treatment of 90° sidewalls.

The concept illustrated in Fig. 1c has been realized in Fig. 7. Figure 7 shows 3D Cu wire distributed on anisotropically etched cavities (200 μm deep) with suspended SiO_2 cantilever arrays. The 3D Cu layer is especially useful for wire routing and interconnection. As a comparison, the existing spray photoresist coating technique is still not available for the substrate with suspended microcantilevers.[6,7] Moreover, the ED technique is only appropriate for the substrate covered with a conductive layer,[2-5] hence, the photoresist will not coat on the SiO_2 cantilever. As a second example, the SEM micrographs in Fig. 8 also show integration of the 3D Cu pattern with suspended structures. The results demonstrate the concept shown in Fig. 1d. These 3D Cu patterns were fabricated using the processes in Fig. 2b2–2e2. During the CDE process in Fig. 2d2, it took 15 and 34 s, respectively, to replace Si by Cu for the substrate with Si–H and Si–H/Si–O bonds on the surface. According to the Cu replacement selectivity between the Si–H, and Si–H/Si–O surfaces, only the Si under the Si–H bond was replaced by Cu^{2+} ions. The Cu pattern (in white) at the bottom of cavity (150 μm deep) was directly transferred from the suspended structure (in gray) using the O_2 plasma. The electrical resistivity of the deposited copper film by CDE plating was about 5.51–6.98 μΩ cm.

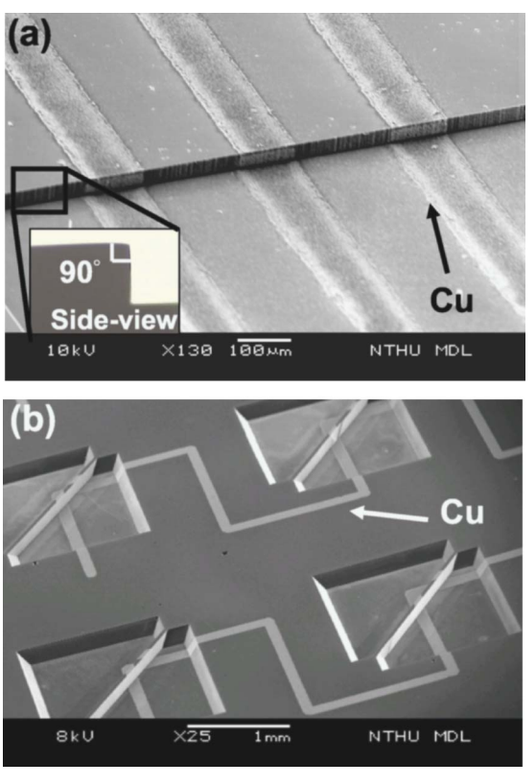

Figure 6. SEM micrographs of 3D Cu patterns distributed on a silicon surface with (a) 90° sidewall cavities and (b) more complicated silicon cavities.

Conclusions

In summary, this study accomplishes 3D lithography on complicated surfaces using SAM coating and plasma treatment. In addition, Cu metallization on a 3D surface and even underneath the suspended microstructures is realized using the CDE plating. The

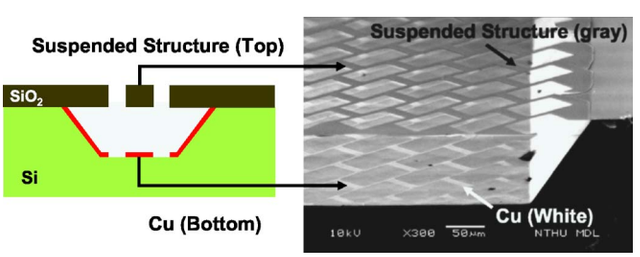

Figure 8. The cross-sectional view of SEM micrographs for 3D Cu patterns distributed on silicon surfaces with underneath the suspended microstructures.

Cu film was conformally plated and patterned on a Si substrate with 50–200 μm deep cavities and 54.7–90° sidewalls. The Cu electrode plated underneath suspended microbeams was also available. The collimation O_2 plasma patterning process was operated in a DRIE system, and its decollimation angle was 0.3–0.7°. Thus, the pattern resolution L is $L = 2h \tan \theta$, where h is the projection distance from the hard mask (in Fig. 2c1) or the suspended structure (in Fig. 2c2) to the surface to be patterned. The collimation of the plasma can be further improved using the ICP system. The adhesion of the copper structures is not good; however, it can be improved by annealing the sample in reducing atmosphere (H_2). The minimum feature size patterned in this study was 20 μm. The alignment was performed using a two-axis (X–Y) linear position stage under an optical microscope. The best alignment accuracy obtained so far was 5 μm. However, the alignment accuracy can be significantly improved using a professional position stage (X–Y–θ) for lithography. Since these are all low-temperature processes, the present concept is easy to integrate with other fabrication technologies. Moreover, the very expensive projection exposure system is not required. In addition, the existing ED and spray technologies are still not able to coat PR on the substrate with suspended microstructures. Furthermore, the 3D lithography on complicated surfaces and even underneath the suspended microstructures can be beneficial to applications in MEMS and in microelectronics as well.

Acknowledgments

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