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A boron etch-stop assisted lateral silicon etching process for improved high-aspect-ratio silicon micromachining and its applications

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Abstract
High-aspect-ratio micromachining (HARM) developed in recent years has made many devices more versatile compared to the surface micromachining process, but it has also met some challenges which have not occurred before. Those issues made many restrictions on HARM structure design, including structure thickness/width limitations, anchor-induced design problems, thickness uniformity and sidewall conductivity problems, which are discussed in this paper. Accordingly, we propose a novel boron etch-stop assisted lateral silicon etching (BELST) process which employs the (111) wafer process and heavy boron diffusion. Many design constraints have been reduced through some delicate designs of the BELST process. Furthermore, the process is capable of various applications, and has been applied in fabricating a dual mass-spring resonator and a micro vibrating gyroscope in this work. In summary, the developed BELST process can possess most existing merits as well as reducing many design constraints in the existing HARM process, and is expected to contribute in making HARM more competitive and convenient.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Single-crystal silicon (SCS) is a good material for microelectromechanical systems (MEMS) devices for its superior characteristics regarding stress-free, compatible coefficient of thermal expansion (CTE) and good mechanical properties [1]. To fabricate SCS microstructures with more design flexibility, high-aspect-ratio micromachining (HARM) has been developed in recent years [2–9]. Basically, these methods use deep reactive ion etching (DRIE) for defining structure depth explicitly and exploit either base-removing or bonding-etching mechanisms for releasing the structures (see figure 1). Due to their capability of fabricating high-aspect-ratio and thick structures, those technologies can possess not only good material but also the ability to satisfy many design requirements. Therefore, silicon bulk-micromachining has become more competitive and can contribute to many MEMS devices.

However, design considerations in HARM might not be so straightforward as in the case of surface micromachining. For example, the planer shape of main structure must be designed in grid or narrow-strip type, as indicated in figure 1. The reasons may come from the structure-forming mechanism [2, 3] or the structure-releasing mechanism [4]. As a result, some applications such as a torsional mirror with good reflective surface or a gyroscope with large effective area will be restricted. Some methods are likely to cope with this problem [5–8], but may still lead to other difficulties, such as anchor-induced design limitation [5], precise fabrication of device thickness [6], or limited diffusion depth [7]. Recently, fabrication of MEMS structures using (111) silicon wafer has been reported extensively [8–12]. A special feature of this process is the lateral silicon etching mechanism, which enables fabrication of a thick, suspended structure with even surface. In addition, the (111) wafer is also ideal for its mechanical isotropy [13], simple process steps and low wafer

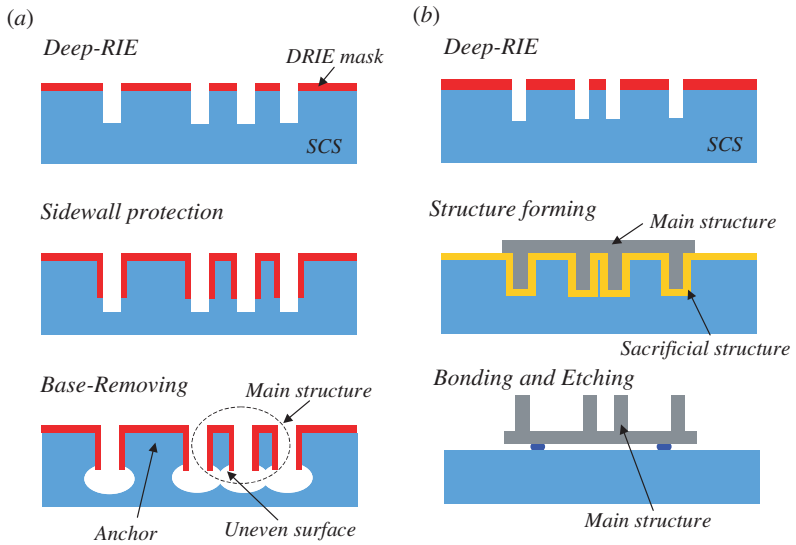

Figure 1. Structure releasing mechanisms of HARM by (*a*) base-removing method, (*b*) bonding-etching method.

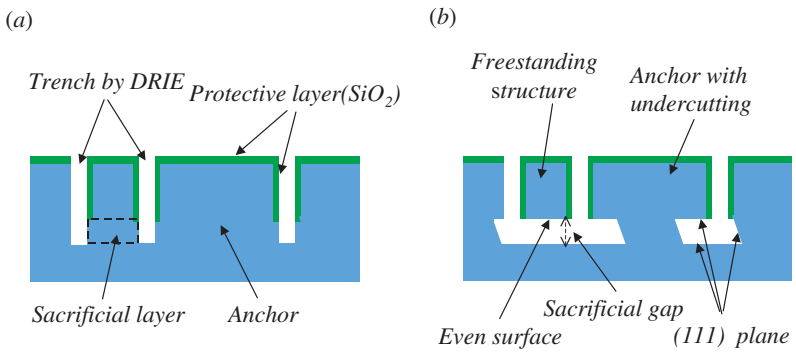

Figure 2. Lateral silicon etching on (111) Si wafer: (*a*) before releasing, (*b*) after releasing.

cost. Though embedded with so many advantages, there are certain limitations which still exist in their fabrication. Accordingly, we propose an improved (111) wafer process to reduce those design constraints, and hopefully to make HARM more competitive and convenient.

In this paper, the existing (111) silicon wafer process is addressed first. After that, a novel 'boron etch-stop assisted lateral silicon etching (BELST) process' is presented. This process can release many design constraints and promote more fabrication capabilities than the existing techniques. Various design concepts have been demonstrated by the fabrication results. Finally, two applications are implemented, including the fabrications of a dual mass-spring resonator and a micro vibrating gyroscope. According to the results, the demands for design can be fulfilled using the developed BELST process.

2. Process exploitation

2.1. (111) Silicon wafer process

The wafer normal aligned to the ⟨111⟩ direction is called the (111) wafer; thus any plane parallel to the wafer surface is also in ⟨111⟩ orientation. Besides, the (111) plane has the slowest etch rate (or etch-stop characteristic) in silicon anisotropic etching using alkaline solution. Accordingly, lateral etching to form parallel and flat surfaces along the sacrificial gap is enabled by these characteristics, as shown in figure 2. This unique characteristic can prevent the uneven surface result indicated in figure 1(*a*), and therefore has the potential to fabricate suspended structures without width limitation. In addition to this, structures fabricated using the (111) wafer can have many device advantages including mechanical isotropy, simple process steps and low wafer cost. However, in applying the (111) silicon wafer process, some other issues that will reduce the design flexibility still exist.

The first issue is regarding the anchor problem during structure releasing. In addition to serving as mechanical support and electrical connection of main structures, anchors must firmly connect to the substrate so that they can sustain the pressure during bonding or probing. In the surface process, the anchor material is different from that of the sacrificial layer; thus can go without any releasing problem. But for the (111) wafer process shown in figure 2(*a*), the anchor material is the same as the sacrificial layer material. Since independent anchors are all with convex corners, they will inevitably suffer from undercutting. The undercutting will start from the corners of the anchors and etch away more material as time goes by. If the releasing time is not properly controlled, the anchors will either be etched away or become too weak to sustain external pressure. Consequently, short

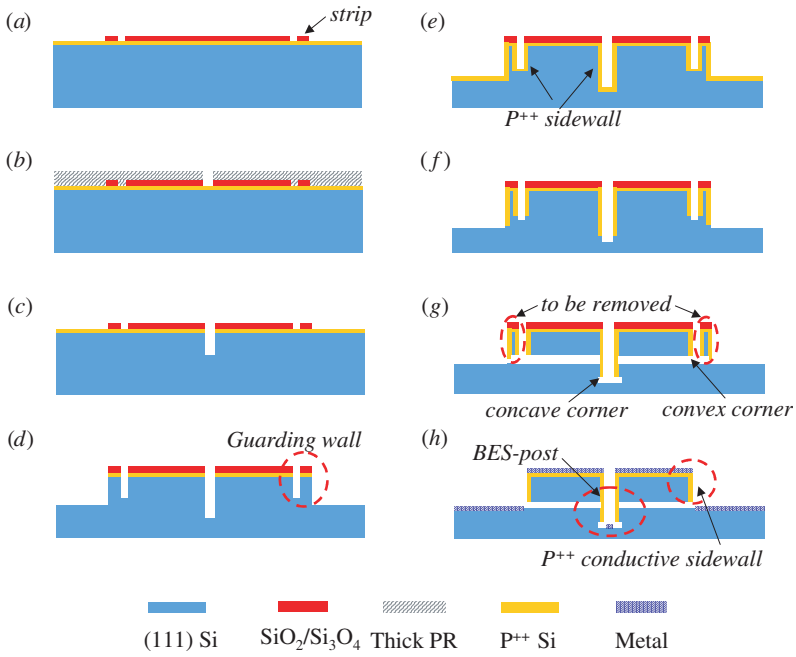

Figure 3. Fabrication sequence of BELST process.

etching time is required and structure width should be set much smaller compared to anchor width, as shown in figure 2(*b*). These limitations will inevitably increase constraints in structure designs.

The other issue is the RIE-lag problem which comes from using DRIE to fabricate high-aspect-ratio structures [14]. Etched depths of different trenches will not be the same if the corresponding etching windows do not have the same width. This situation may be much worse in very deep trench etching. Therefore, some unwanted results after the releasing step might occur, including the irregular shapes of spring and mass element. In other words, to obtain equal etched depth without special treatments on the facility, equal line-separation is preferred in the mask design. However, this design may confine the moving part and cause the parasitic capacitance problem. Decreasing the etching depth may improve the thickness uniformity, but will also increase the design constraints.

The requirement of high conductive sidewall in high-aspect-ratio structures is still an issue. Diffusing the dopant to produce a conductive thickness in the vertical direction was used in [7, 8]. However, junction depth in acceptable diffusion time is highly limited, which restricts the height of the conducting sidewall. For depositing conductive material such as aluminum onto the tall and steep sidewall, special adjusting of the metal PVD parameters is needed [4]. Besides, uniformity may still depend on the etched depth and width of etching opening. In [9], the bilayer film consisted of conductive CVD poly-Si and the thermal SiO_2 layer was used for dissolving the sidewall limitation. This method can indeed increase the conducting height to an extent due to good step coverage of LPCVD films. However, in some cases such as device packaging or sensing electrode combination where the bonding process might be needed, carrying out the sequential bonding does not seem easy for this process.

All the mentioned challenges seldom met in the surface process come from the need for stable fabrication for thick/wide freestanding structures in MEMS devices. To overcome the mentioned problems, this study modifies the existing (111) silicon wafer process and proposes a novel BELST process, as stated in the next section.

2.2. BELST process

To alleviate the problems mentioned in the last section, a modified (111) silicon wafer process is proposed, called the BELST process. The sequence of this two-mask fabrication process is shown in figure 3, which uses n-type (111) silicon wafer as the substrate. The process begins with boron diffusion to enable conductivity of the wafer surface, and then SiO_2/Si_3N_4 film as the DRIE mask is deposited and patterned as in figure 3(*a*). In the patterning step, many strips are defined in the peripheral of the main structures, which will form the guarding wall in later process indicated in figure 3(*d*). After that, thick photoresist (PR) which served as the second DRIE mask is spun and patterned, as shown in figure 3(*b*). The reason for using two DRIE masks is to generate two different etched depths which enable the fabrication of the boron etch-stop-post (BES-post) indicated in the final result (figure 3(*h*)). As in figures 3(*c*)–(*e*), two DRIE steps to define the structure thickness are then followed, and are continued by heavy boron diffusion to form a protective/conductive P^{++} sidewall (also indicated in figure 3(*h*)). After that, a third DRIE step shown in figure 3(*f*) is performed to etch away the bottom p^{++} silicon and define the thickness of the sacrificial layer. Finally, lateral silicon etching in alkaline solution is carried out and freestanding structures are then released, as shown in figure 3(*g*). Note that the DRIE etching window at the center of the structure is set to be a hole with concave corners only, which

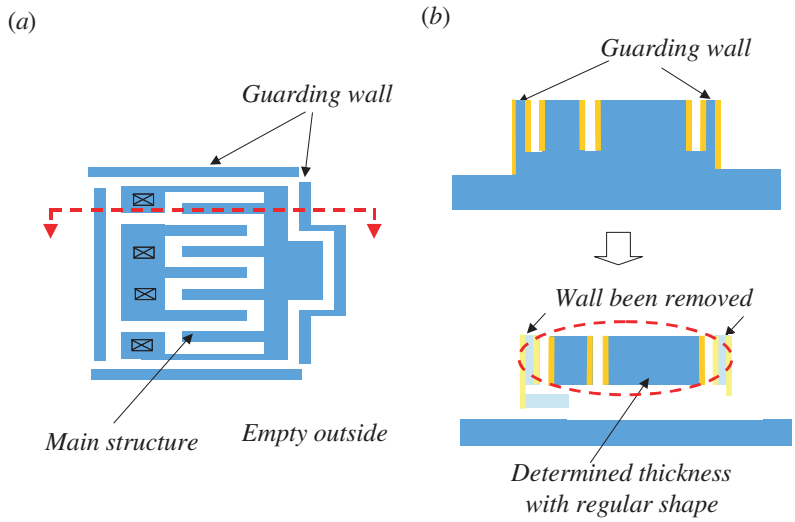

Figure 4. Schematic drawing of guarding-wall design: (*a*) top view, (*b*) side view.

will prevent the convex corner undercut effect. Therefore, lateral silicon etching that needs undercutting will be carried out only at the surroundings of the main structures but not at the central part where the BES-post stands. Further process steps, such as bonding, selective oxidation or metallization, can be executed according to the demands as in figure 3(*h*). Compared with the traditional (111) silicon wafer process, the proposed BELST process does have several salient features, which are described below.

As mentioned in section 2.1, traditional equal line-separation design for reducing RIE-lag will lead to the main structures being confined by the enveloping walls. These walls are likely to introduce more parasitic capacitance. To cope with the RIE-lag as well as the enveloping wall problem, the design of the guarding wall indicated in figure 3(*d*) is proposed, whose principle is shown in figure 4(*a*). Only inside guarding walls should line separation be obeyed. Therefore, within guarding walls, all trenches will be etched at the same depth, which guarantees the main structures with the same thickness, as shown in figure 4(*b*). After releasing, the guarding walls affected by RIE-lag will be removed since they are not connected to any anchors. Therefore, it will not influence the main structure. With this attempt, structures with precise thickness and regular shape can be obtained. On the other hand, the parasitic capacitance can be decreased.

A versatile BES-post can be fabricated, as shown in figure 3(*h*). Inside the BES-post, undercutting will stop at the hexagonal pits bounded by the (111) planes due to concave corner. Outside the BES-post, the silicon sacrificial layer will be etched away and then structures will be released. One promising application of the BES-post is corner compensation of anchor undercutting, a proper solution for the mentioned anchor problem. Referring to figure 5(*a*), although the shape of the anchor is hexagon with one edge aligned to the ⟨111⟩ direction, it will still suffer from undercutting due to the convex corner effect. The corner compensation method for the anchor on the (111) silicon wafer has been proposed in [8]. However, this approach still requires extra occupied space and special care for etching time. Accordingly, a BES-post compensation method is proposed here, which utilizes the etch-stop property of the BES-post and (111) wafer crystallization. As shown in figure 5(*b*), the method is by arranging BES-posts in the adjacent of convex corners to suppress the corner undercut effect. Since the corners and sides are protected by BES-post and (111) plane, respectively, nowhere beneath the anchor would be penetrated during releasing. Therefore, corner compensation without extra area and relatively small anchors can be reached. Moreover, since the tolerable etching time can be very long, wide structures on (111) wafer can still be realized. In addition to corner compensation, the BES-post can be applied in many other occasions, which are shown in the next section.

As indicated in figure 3(*e*), a uniformly diffused P^{++} sidewall is used instead of traditional SiO_2 film as the sidewall protective material. This sidewall not only serves as a protection layer for wet etching, but also offers the essential electrical conductivity, which solves the limitation of conductive-sidewall height described in section 2.1. In addition, different from the etch/diffusion process [3], this lateral diffusion step need not completely convert the entire 'width' of the structure to p^{++} type. The reason is that the bottom surfaces of structures are protected by the (111) plane and will not be attacked. Therefore, the structure width limitation of that method is also dissolved. To accomplish the electrode isolation, the p–n junction isolation technique [3, 8] is adopted here to isolate different electrodes. As shown in figure 6, body bias V_{bias} is set larger than driving voltage V_{drive}, which forces the p–n junction in the reverse-bias condition. A thick depletion layer surrounding all structures will be induced, and can then serve as a good insulation layer for isolation.

Moreover, BELST could have the flexibility in making many extended processes. For example, the Si_3N_4 film on top surface can serve not only as an etching barrier but also as an oxidation barrier for selective oxidation. Therefore, oxide film selectively growing on conductive sidewall can be performed in the BELST process. The SiO_2 layer on sidewalls, whose permittivity is larger than air, can possess two advantages. One is the enhanced electrostatic driving/sensing ability due to decreased equivalent gap of capacitance. The other is the ability to compensate the spring thickness which is consumed during the photolithography, ICP-RIE and releasing processes.

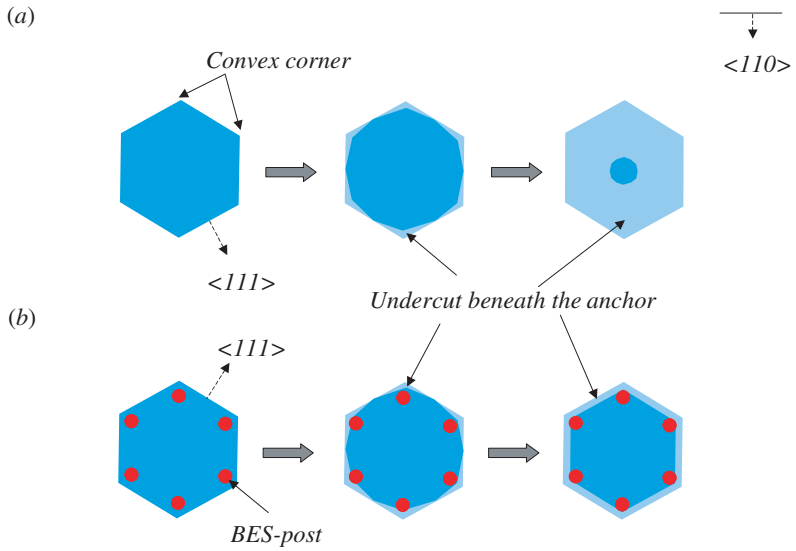

Figure 5. Undercut of a hexagon anchor on (111) Si wafer: (*a*) without corner compensation, (*b*) compensated by BES-post.

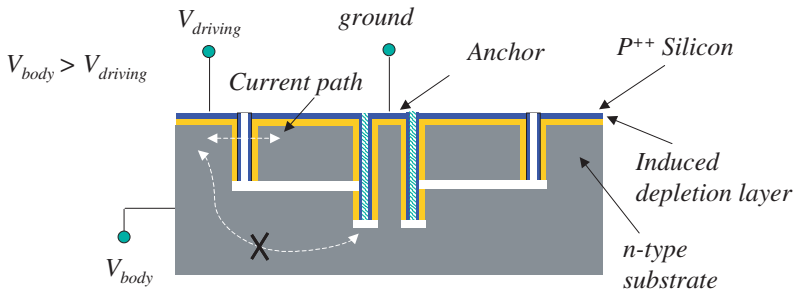

Figure 6. Isolation technique of the BELST process, using the p–n junction isolation method.

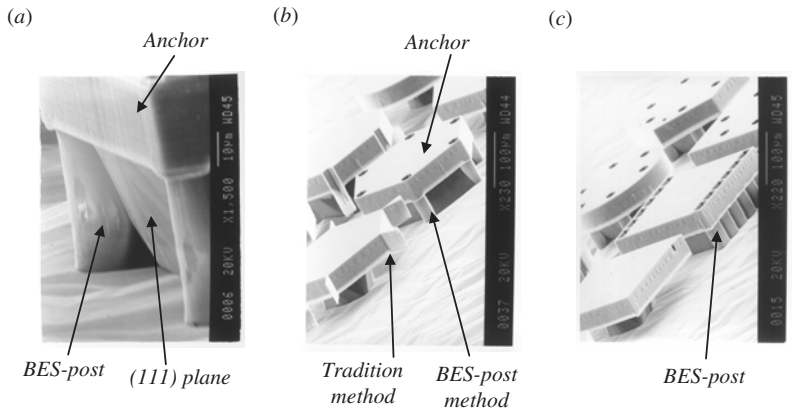

Figure 7. BES-post corner compensation results: (*a*) close-up view of the BES-post, (*b*) hexagon anchor, (*c*) non-hexagon anchor.

Therefore, the post tuning of system characteristics such as resonance frequency is possible. Another example is wafer bonding. After removing the SiO_2/Si_3N_4 film, the conductive top surface will be exposed. Due to good surface roughness condition in BELST process, the electrical connection through metalization or wafer bonding [15] from the top surface could be carried out. Various wafers could bond, including a glass wafer with sensing electrodes or a silicon wafer with a circuit on it. Therefore, many extending processes are available and could provide more design flexibility.

2.3. Process results

Figure 7 shows the BES-post corner compensation results. From the close-up view of the BES-post in figure 7(*a*), we can see that undercutting was stopped by the (111) plane and BES-post, which proves the idea of compensation using the proposed method. To compare, results of corner compensation using traditional and BES-post methods are shown in figure 7(*b*). Undercutting in the former case depended on the etching time, while the situation could be avoided in the latter case. Moreover, for the anchor whose shape is not hexagon, the

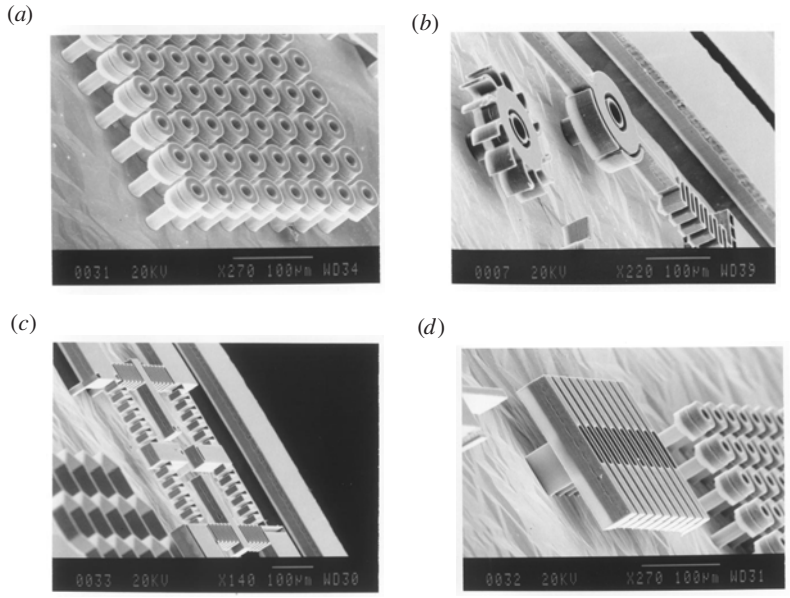

Figure 8. Passive components fabricated along with the BES-post: (*a*) array with vertical spring, (*b*) pivot, (*c*) suspended structure, (*d*) thermal isolation platform.

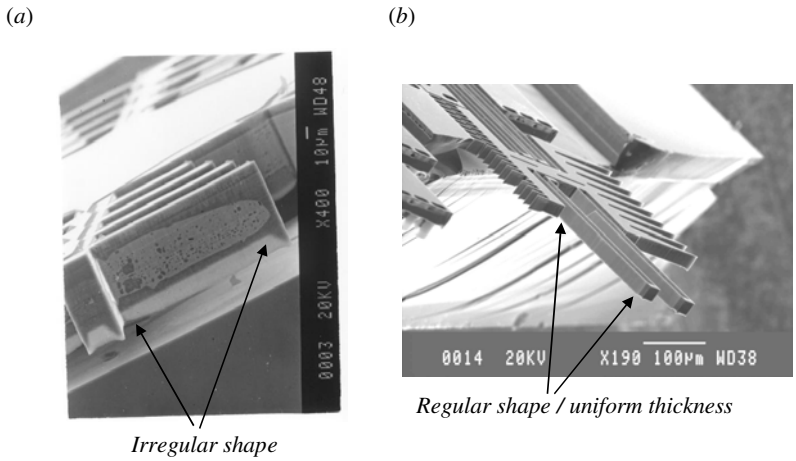

Figure 9. Comparison for structures fabricated with and without guarding wall.

compensation effect can still be obtained by applying adequate BES-posts to enhance the non-⟨111⟩-oriented side, as shown in figure 7(*c*). Some passive structures exploiting the BES-post are also shown in figure 8, which reveals the potential in exploiting the BES-post. Note that if the BES-post is deep enough, less influence on the suspended structure could be expected.

To compare the uniformity, the fabrication result of structures without using a guarding wall is shown in figure 9(*a*). The irregular shape and thickness will occur not only in the main structures but also in the spring element, and both will substantially deteriorate device performances. By applying guarding-wall design, regular shape along with good thickness uniformity could be obtained, as shown in figure 9(*b*). In addition, we can see that no enveloping wall appeared in the result, which is advantageous for reducing parasitic capacitance.

The photograph shown in figure 10 is a typical fabrication result for an electrostatic rotary actuator. The anchor located in the center is so small that more space can be left for longer spring design. The sidewalls, whose thickness reaches the design value of 30 μm, are all conductive due to the contribution of P^{++} sidewall. According to the preliminary driving test, the actuators can show significant motion with applied voltage below 20 V. This result proves not only the result of thick conductive sidewall, but also the feasibility of using p–n junction isolation to isolate different electrodes.

3. Applications of BELST process

3.1. Dual mass-spring resonator (DMSR)

3.1.1. Description. For many resonance-type MEMS devices, having large dynamic response is quite desirable. For example, a micro gyroscope with large reference vibration and a scanning mirror with large scanning angle are both desired to obtain better performance. Various methods have been employed to achieve this goal, including the 2-DOF vibration-amplify mechanism [16–18]. Basically, this mechanism consists of two mass-spring vibrating systems connected to

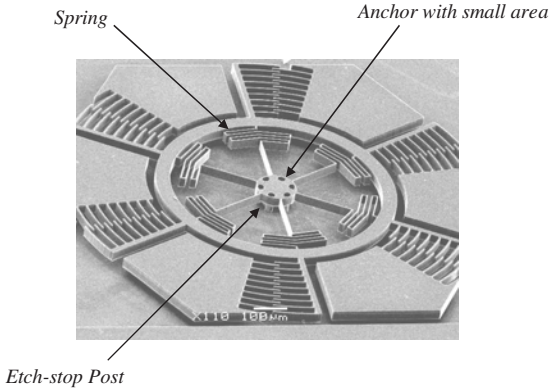

Figure 10. Fabrication result for an electrostatic rotary actuator.

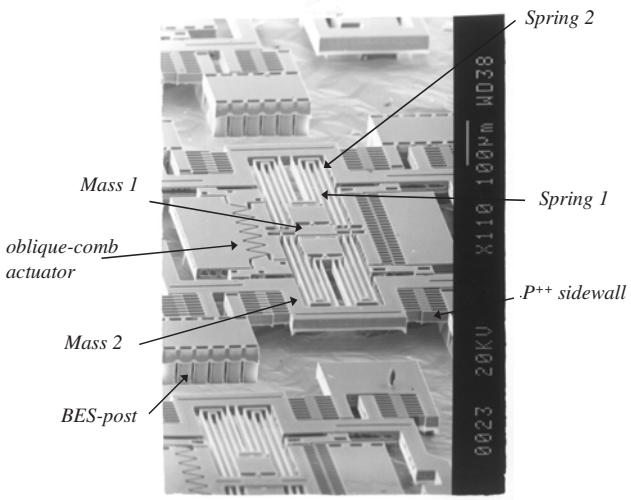

Figure 11. Fabrication result of DMSR integrated with oblique-comb actuator.

each other. The primary reason to use this is that the large output amplitude of one mass-spring system can be driven by the small vibration of the other system. Therefore, those actuators capable of large force could be used to generate the small vibration with less input efforts.

However, an in-plane DMSR cannot be easily implemented using the surface process. One reason is that the effective spring length of DMSR has to be very long, which may lead to sticking problems for processes with limited sacrificial layer thickness [17]. Besides, any external disturbance may cause unwanted motions due to small out-of-plane stiffness. In short, a thick structure as well as large sacrificial gap is needed for in-plane DMSR. As a result, the BELST process seems to be a better choice than the surface process. In addition to suppressing unwanted out-of-plane motions, driving and sensing efficiencies can also be improved, due to thick structures with P^{++} sidewall. Moreover, a minimum occupied space of resonators is expected because of small anchor capability in the BELST process.

3.1.2. Design and fabrication result. According to [18], the first resonance mode of the 2-DOF system is exploited in DMSR design. Meanwhile, a novel oblique-comb actuator is also proposed in order to meet some special

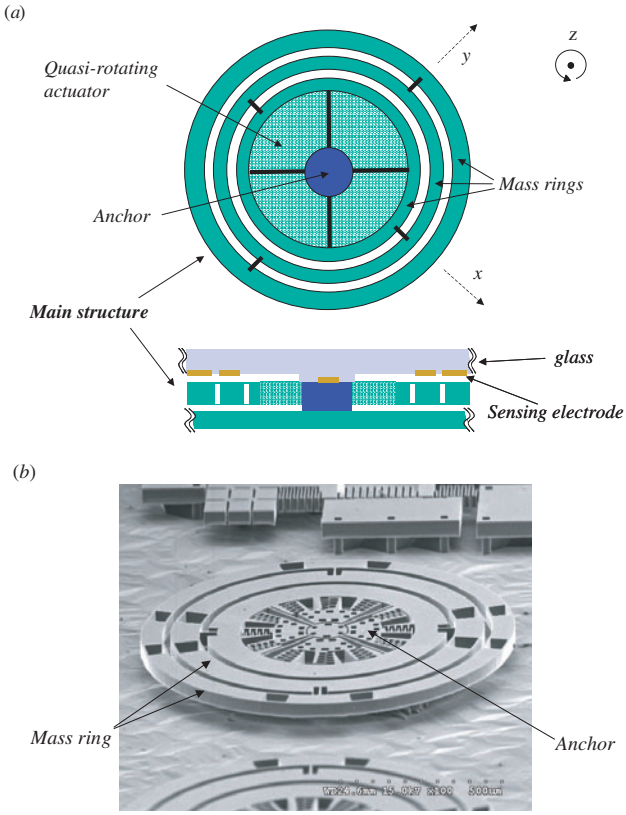

Figure 12. Dual-axis MVG: (*a*) the design, (*b*) fabrication result.

actuator requirements. This actuator with trapezoidal comb fingers can offer flexibility in making a trade-off between allowable stroke and force. In addition, it can easily be implemented using the BELST process. Therefore, a DMSR with large amplitude is then constructed by integrating an oblique-comb actuator into the 2-DOF system. To demonstrate the above concept, test devices were fabricated using the BELST process. In releasing the devices, etching time was not carefully controlled due to BES-post corner compensation design. Besides, no sticking occurred for all the fabricated high-aspect-ratio devices. The fabrication result of the DMSR integrated with the oblique-comb actuator is shown in figure 11. In driving the in-plane resonator, no out-of-plane motion was observed. Motions of the two mass-spring systems could be observed by comparing their blur length during the driving test. The result revealed good motion-amplify effect and output amplitude larger than 30 μm.

3.2. Micro vibrating gyroscope (MVG)

3.2.1. Principle and requirement. Most existing micromachined vibrating gyroscopes measure the angular rate by detecting the corresponding Coriolis force. However, the Coriolis force is so tiny that researchers have to make lots of efforts, such as mechanical responsivity improvement and operating noise reduction, in order to detect this quantity. To attain these goals, care must be taken in the gyroscope structure design. Since the Coriolis force is proportional to the vibrating mass, the vibrating element should have large thickness along with large effective area [19], which can be realized by the BELST process. Its thick structure

capability can further reduce the cross-axis sensitivity and operating noise such as the random shock [9, 20]. Moreover, thick structures with P^{++} sidewall will contribute to large sensing area of capacitance, thus electrical sensitivity can be improved. Therefore, the BELST process embedded with good fabrication flexibility could be then applied in the MVG fabrication.

3.2.2. Dual-axis MVG design and fabrication. According to the requirements, a dual-axis MVG design shown in figure 12(*a*) is proposed. In this design, *z*-axis quasi-rotation is served as the reference motion, and tilting with respect to *x*- or *y*-axes will be the corresponding sensing motion. The three mass rings are designed with large effective area to offer large mass moment of inertia. Through some calculations, proper parameters to meet the frequency-matching requirement of MVG were obtained. Since there are no more limitations regarding ring width/thickness, the design could be relatively straightforward. Output tilting angle will be picked up through sensing electrodes on glass and an external read-out circuit.

Accordingly, the silicon parts of the dual-axis MVG have been fabricated using the BELST process, as shown in figure 12(*b*). Many design features have been successfully realized and can be investigated clearly. The structure thickness was up to 35 μm with good uniformity, due to the use of the guarding wall. The anchor made from the BES-post method was so small compared to mass rings, but could still survive and was strong enough to endure external probing pressure according to our testing. The structures were thick enough to filter out many error sources from the out-of-plane direction. The P^{++} sidewall might also have good conductivity according to the driving test of the quasi-rotating actuator in the center. Besides, the effective area of the mass rings was very large, which can increase the mechanical responsivity and improve the performance of the MVG. The integration with sensing electrodes and capacitance read-out circuit is ongoing and good response is expected according to the fabrication result of mechanical parts.

4. Conclusion

In this paper, a novel BELST process is proposed to improve the fabrication flexibility of HARM. The restrictions in the HARM process, including structure thickness/width limitation, anchor-induced design problem, thickness uniformity and sidewall conductivity problem, can all be reduced using the developed process. The fabrication of a DMSR and a MVG could further demonstrate that the BELST process is qualified for various applications. In summary, the developed BELST process can possess most existing merits as well as reduce many design constraints in the existing HARM process, and is expected to contribute in making HARM more competitive and convenient.

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