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Design and application of a metal wet-etching post-process for the improvement of CMOS-MEMS capacitive sensors

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Abstract
This study presents a process design methodology to improve the performance of a CMOS-MEMS gap-closing capacitive sensor. In addition to the standard CMOS process, the metal wet-etching approach is employed as the post-CMOS process to realize the present design. The dielectric layers of the CMOS process are exploited to form the main micro mechanical structures of the sensor. The metal layers of the CMOS process are used as the sensing electrodes and sacrificial layers. The advantages of the sensor design are as follows: (1) the parasitic capacitance is significantly reduced by the dielectric structure, (2) in-plane and out-of-plane sensing gaps can be reduced to increase the sensitivity, and (3) plate-type instead of comb-type out-of-plane sensing electrodes are available to increase the sensing electrode area. To demonstrate the feasibility of the present design, a three-axis capacitive CMOS-MEMS accelerometers chip is implemented and characterized. Measurements show that the sensitivities of accelerometers reach 11.5 mV G^{-1} (in the *X*-, *Y*-axes) and 7.8 mV G^{-1} (in the *Z*-axis), respectively, which are nearly one order larger than existing designs. Moreover, the detection of 10 mG excitation using the three-axis accelerometer is demonstrated for both in-plane and out-of-plane directions.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

CMOS-MEMS capacitive sensors have been widely used to detect the changes of various physical quantities such as acceleration [1–3], humidity [4], angular rate [5], etc. Presently, many studies are being reported to improve the performance of capacitive-type CMOS-MEMS sensors. A very straightforward approach is to optimize the design of mechanical components, such as the spring stiffness and mass. For instance, the proof-mass of the accelerometer in [6] is increased by means of the post-CMOS process, and the sensitivity of the accelerometer is also increased. Moreover, the study in [7] reports the concept to increase the number of sensing electrodes so as to increase the sensing capacitance of the accelerometer. The designs of capacitive sensing electrodes, such as the gap of gap-closing electrodes [8] and the overlap area of comb-type electrodes [9], etc, are also effective approaches to improve the performance of the capacitive type sensors.

The in-plane sensing gaps of the existing capacitive-type CMOS-MEMS sensors are usually defined by anisotropic dry-etching processes such as RIE and DRIE (reactive ion etching)

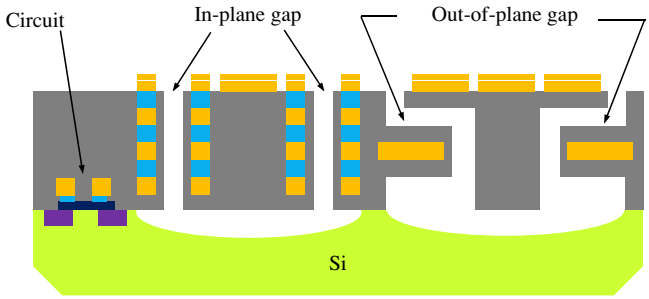

Figure 1. Cross-sectional view of the CMOS-MEMS gap-closing capacitive sensors with in-plane and out-of-plane sensing electrodes.

[1–3, 5]. These dry-etching processes can provide clean and directional structure geometry. However, such etching approaches are also accompanied by some disadvantages: (1) the aspect ratio of RIE etching and the thickness of the thin film structure limit the width of the in-plane sensing gap. For instance, it is difficult to achieve a sub-micron gap for the MEMS structure fabricated using the commercial TSMC 2P4M (formed by two poly-Si and four metal and dielectric layers, in total nearly 7 μm thick) CMOS process; (2) the metal layer is required to act as the hard mask for the RIE etching process. Thus, the metal hard mask and the metal layers underneath (such as the routing wires and the sensing circuits) will introduce the parasitic capacitance C_p. The C_p would couple with the sensing capacitance and further reduce the sensitivity and resolution of capacitive sensors [10]; and (3) the undercut of the metal layer to define the out-of-plane sensing gap is not available for the anisotropic dry-etching process.

Moreover, the wet-etching approach has been employed to fabricate the out-of-plane sensing gaps of various capacitive sensors [11]. In this regard, the metal films, including the aluminum and tungsten vias, are employed as the sacrificial layer. This study exploits the existing sacrificial metal wet-etching approach to define the in-plane as well as out-of-plane sensing gaps for CMOS-MEMS gap-closing capacitive sensors. The width of in-plane sensing gap determined by the wet-etching process will not be influenced by the aspect ratio of the structure. Thus, sensing electrodes with sub-micron in-plane as well as out-of-plane sensing gaps can be achieved. Moreover, the metal hard mask for dry etching is not required, so that the parasitic capacitance is reduced. As a result, the present design significantly improves the sensitivity and resolution of the CMOS-MEMS gap-closing capacitive sensor.

2. Fabrication process and design

Figure 1 shows the cross section of typical in-plane and out-of-plane gap-closing capacitive sensors. These gap-closing capacitive sensors mainly consist of stationary and movable sensing electrodes. There is a sensing gap between the stationary and the movable sensing electrodes. As indicated in figure 1, the displacement of the movable electrode will cause a capacitance change between the sensing electrodes.

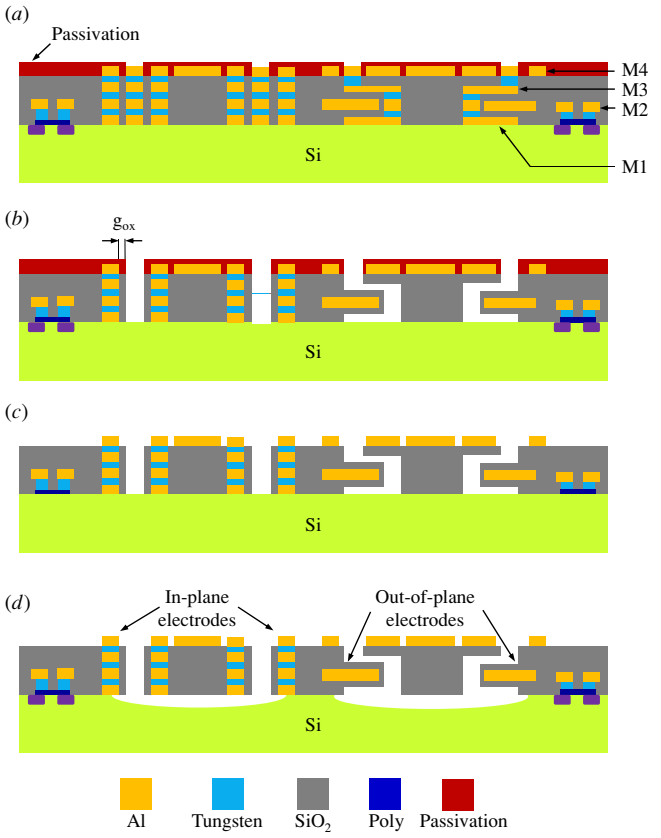

Figure 2. The fabrication process steps: (*a*) CMOS chip fabricated by the TSMC 0.35 μm 2P4M CMOS process, (*b*) metal wet etching to form the in-plane and out-of-plane gaps, (*c*) RIE to remove the passivation, and (*d*) XeF_2 silicon substrate isotropic etching to release the MEMS structures.

In general, the capacitance change ΔC of the gap-closing electrodes with the overlap sensing area of A, and the initial sensing gap d can be expressed as [7]

$$\Delta C = \frac{\varepsilon A}{d - \Delta d} - \frac{\varepsilon A}{d + \Delta d} \approx \frac{2\varepsilon A}{d^2}\Delta d, \qquad (1)$$

where Δd is the variation of sensing gap, and ε is the dielectric constant of the material between the sensing electrodes. Based on the concept of reducing the sensing gap as well as increasing the overlap area of sensing electrodes, this study has designed and implemented higher sensitivity CMOS-MEMS gap-closing capacitive sensors using the metal wet-etching post-CMOS process. Moreover, this study also presents an approach to reduce the parasitic capacitance of the sensors using the metal wet-etching post-CMOS process.

2.1. Fabrication process

Based on a commercial 2P4M (two polysilicon, four metal and dielectric layers) CMOS process, this study presents the metal wet-etching approach illustrated in figure 2 to fabricate sensing electrodes with a sub-micron sensing gap and a larger sensing area. Firstly, the CMOS chip is fabricated by the standard TSMC 0.35 μm 2P4M CMOS process, as illustrated in figure 2(*a*). The four metal layers are labeled as M1–M4.

In addition to the in-plane and out-of-plane capacitance-sensing element, the sensing circuits are also embedded in this chip. The figure clearly shows the pattern and stacking of metal and dielectric films designed by the present study. As shown in figure 2(*b*), the wet-etching process was employed to remove the sacrificial metal layers including the aluminum films and the tungsten vias. Thus, the in-plane shapes of the mechanical components, such as the spring and mass, and the sensing electrodes and sensing gaps were defined. In addition, the out-of-plane sensing electrodes and sensing gaps were also defined in this manner. During the metal wet-etching process, the structure and sensing electrodes were protected by the dielectric layers of the CMOS process. Meanwhile, the sensing circuit and bonding pads were protected by the passivation layer. The etching selectivity between the dielectric film and metal layers during the wet etching is extremely high, so that the MEMS structures and the sensing gaps can be precisely defined. As shown in figure 2(*c*), after the metal wet etching, RIE was used to remove the passivation to expose the metal bonding pads formed by the M4 layer. The mechanical structures and sensing electrodes were finally released from the substrate after isotropic silicon etching by XeF_2, as shown in figure 2(*d*).

2.2. Sub-micron sensing gaps

As limited by the aspect ratio of the dry-etching process, the sensing gaps can only reach 1.5 μm for the 7 μm thick 2P4M CMOS-MEMS structure when defined by the RIE process [7]. As shown in figures 2(*a*)–(*b*), this study employs the metal films and tungsten vias as sacrificial layers, and to define the sensing gaps by metal wet etching. According to the CMOS process design rule, the minimum line widths of the metal and via layers are 0.6 μm and 0.5 μm, respectively, which are much smaller than that defined by dry-etching approaches. Since the metal sensing electrodes are covered and protected by the dielectric film, the equivalent in-plane sensing gap g_{eff}, is yielded as

$$g_{\text{eff}} = \frac{2g_{\text{ox}}}{\varepsilon_{\text{ox}}} + \frac{g_{\text{air}}}{\varepsilon_{\text{air}}}, \tag{2}$$

where g_{ox} is the thickness of the protection dielectric film on the sidewalls of the electrodes (as indicated in figure 2(*b*)), and g_{air} is the width of the sensing gap defined by the sacrificial metal layer. The effective sensing gap is significantly reduced by nearly 50% as compared with that defined by dry etching. Thus, the sensitivity of the capacitive sensor can be increased twofold in this manner.

The out-of-plane gap is also designed using the same concept, as shown in figures 2(*a*)–(*b*). In this case, the M2 and M4 metal layers are respectively exploited as the bottom and top electrodes. The M3 metal layer acts as the sacrificial layer to define the sensing gap between the top and bottom sensing electrodes. The thickness of the M3 layer is 0.64 μm; thus a sub-micron out-of-plane sensing gap can be achieved. In short, the metal wet-etching approach exploits the characteristic of fine line width of the CMOS process to improve the performance of capacitive sensors. The sensing gap and sensitivity of the capacitive sensor can be further improved by other advanced CMOS processes with even smaller minimum line width.

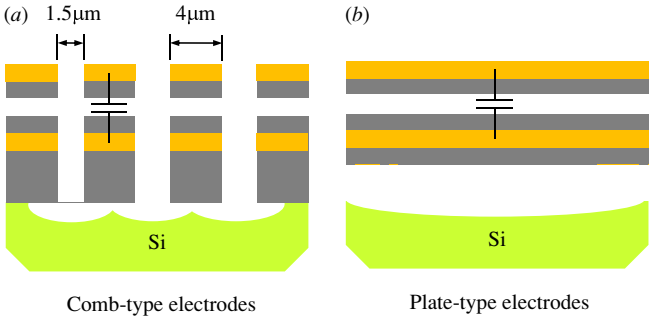

Figure 3. (*a*) The comb-type out-of-plane sensing electrodes, and (*b*) the plate-type out-of-plane sensing electrodes.

2.3. Large area out-of-plane sensing electrodes

Figure 3(*a*) shows the comb-type sensing electrodes for out-of-plane sensing in [8]. This study employs the metal wet-etching process to fabricate the plate-type sensing electrodes, as indicated in figure 3(*b*), to increase the sensing area of the electrodes. In this regard, the M1 metal layer is also exploited as a sacrificial layer. The isotropic metal wet etching is performed along the path consisting of M1 layer, M3 layer and tungsten via. As indicated in figure 2(*c*), the bottom electrode formed by the M2 metal film is fully suspended after the etching of the M1 sacrificial layer. According to the extremely high selectivity, the dielectric film is rarely attacked during the undercut of the M1 layer. Meanwhile, the silicon substrate underneath the plate-type sensing electrodes is fully exposed. Thus, as shown in figures 2(*d*) and 3(*b*), the XeF_2 etching of the silicon substrate underneath the sensing electrodes can easily and rapidly proceed, despite the large area of plate-type sensing electrodes. In comparison, as shown in figure 3(*a*), the comb-type electrodes design is required to properly undercut the silicon substrate if the M1 layer is not removed. For a typical dry-etching approach in [8], a 1.5 μm spacing between the pair of sensing fingers is required to remove the 7 μm thick dielectric layers by RIE to expose the silicon substrate underneath. Moreover, to prevent the large silicon substrate undercut during the following XeF_2 etching, the width of the pair of sensing fingers is designed to be 4 μm. As compared with the comb-type sensing electrodes in [8], the plate-type design realized by the metal wet etching increases the fill factor by 37.5%.

2.4. Elimination of parasitic capacitance

Figure 4 shows the detailed concept of the present study regarding the elimination of parasitic capacitance for sensing circuit and routing wires. The left illustration shows the conventional design with top metal layer as the hard mask to protect the sensing circuits and routing wires underneath during the RIE etching. Thus, the metal hard mask forms the parasitic capacitance C_p with the metal layers underneath, as indicated in the figure. The parasitic capacitance will influence

Table 1. The specifications of the three-axis accelerometers realized using the present approaches, and comparison with existing designs.

Specifications	*X* & *Y* [1]	*Z* [2]	*X* & *Y* [7]	*Z* [8]	*X* & *Y*	*Z*
Range (G)	0.1–13	0.5–27	0.3–10	0.5–5	0.01–3.0	0.01–3.0
Sensitivity (mV G^{-1})	0.5	0.5	3.95	1.14	11.5	7.8
Noise (mG $Hz^{-1/2}$)	1	6	100	N/A	2.4	4.1
Cross-axis (%)	5	5	<5	N/A	1.7	0.12
Nonlinearity (%)	N/A	N/A	2.75	3.4	0.5	3.7

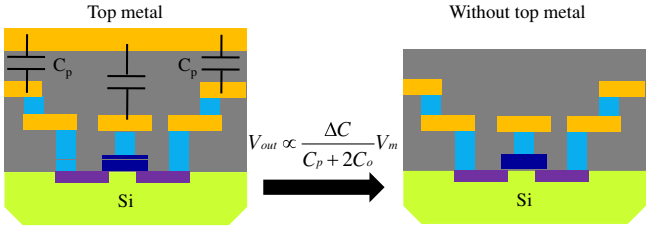

Figure 4. The elimination of parasitic capacitance after removing the top metal layer.

the performance of the capacitive sensor; for instance, the gain of the capacitive accelerometer in [10] varies with the parasitic capacitance C_p as

$$\text{Gain} \propto \frac{1}{(C_p + 2C_0)},$$

where C_0 is the sensing capacitance of the sensor. Since the dielectric constant of the SiO_2 layer is fourfold higher than that of air, the parasitic capacitance indicated in the left illustration of figure 4 cannot be ignored. The right illustration of figure 4 shows the present design where the top metal layer that acts as the hard mask is not required for the post-CMOS process. Thus, the parasitic capacitance C_p is eliminated to improve the performance of the capacitive sensor.

3. Experiment and results

A capacitive three-axis CMOS-MEMS accelerometer chip has been employed to demonstrate the feasibility of the present design. As illustrated in figure 5(*a*), the sensing chip contains two in-plane (*X*-axis and *Y*-axis) and one out-of-plane (*Z*-axis) accelerometers. The in-plane and out-of-plane gap-closing sensing electrodes illustrated in figure 1 are respectively employed for the in-plane and out-of-plane accelerometers. The zoom-in illustration in figure 5(*b*) shows the plate-type gap-closing sensing electrodes design of the out-of-plane accelerometer. The fully differential sensing electrodes designs are also available in all three-axis accelerometers. The mechanical components, such as the mass and spring, for both in-plane and out-of-plane accelerometers are mainly made of the CMOS dielectric material (SiO_2). The metal films and tungsten vias are only employed as the routing wires and sensing electrodes.

3.1. Fabrication results

The SEM micrographs in figure 6 show the typical fabrication results of the three-axis accelerometer. Figure 6(*a*) shows

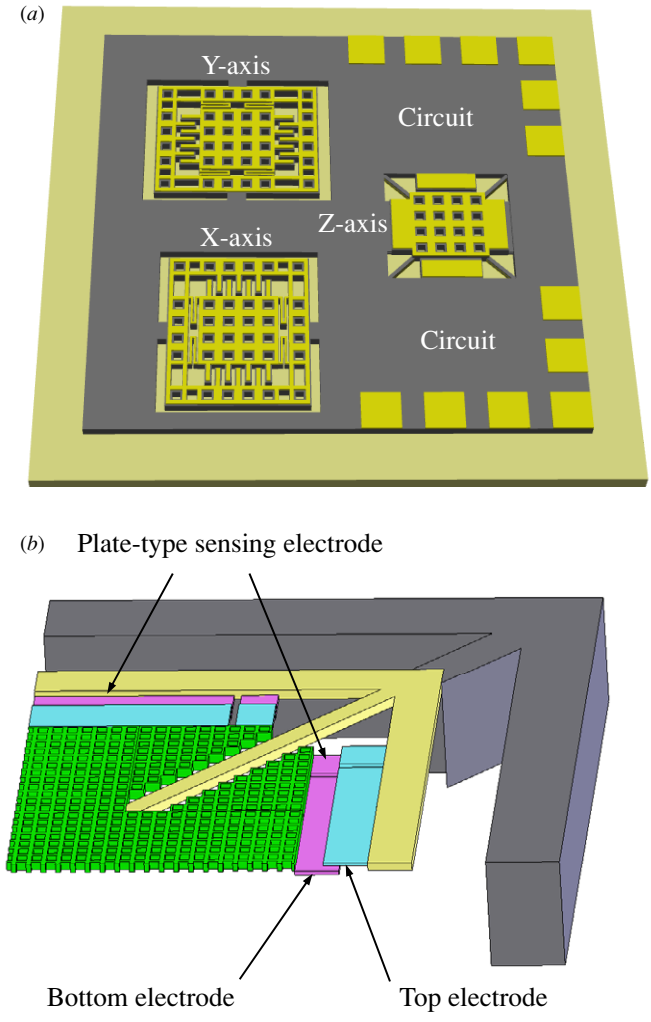

Figure 5. (*a*) The CMOS chip containing three-axis accelerometers used to demonstrate the present capacitive sensor design; (*b*) zoom-in of the *z*-axis accelerometer to show the plate-type sensing electrodes.

the three-axis accelerometer consisting of two in-plane (*X*-axis and *Y*-axis) and one out-of-plane (*Z*-axis) accelerometers. Figure 6(*b*) shows the in-plane accelerometer. A pair of the in-plane sensing electrodes is highlighted by the zoom-in micrograph in figure 6(*c*). The measured in-plane sensing gap was 780 nm, which was larger than the designed value of 600 nm. Nevertheless, such a sub-micron in-plane sensing gap cannot be achieved by the dry-etching process. Figure 6(*d*) further shows the cross-sectional view of the sensing electrodes. The bright region is the sensing electrodes consisting of the metal films and tungsten vias, and the

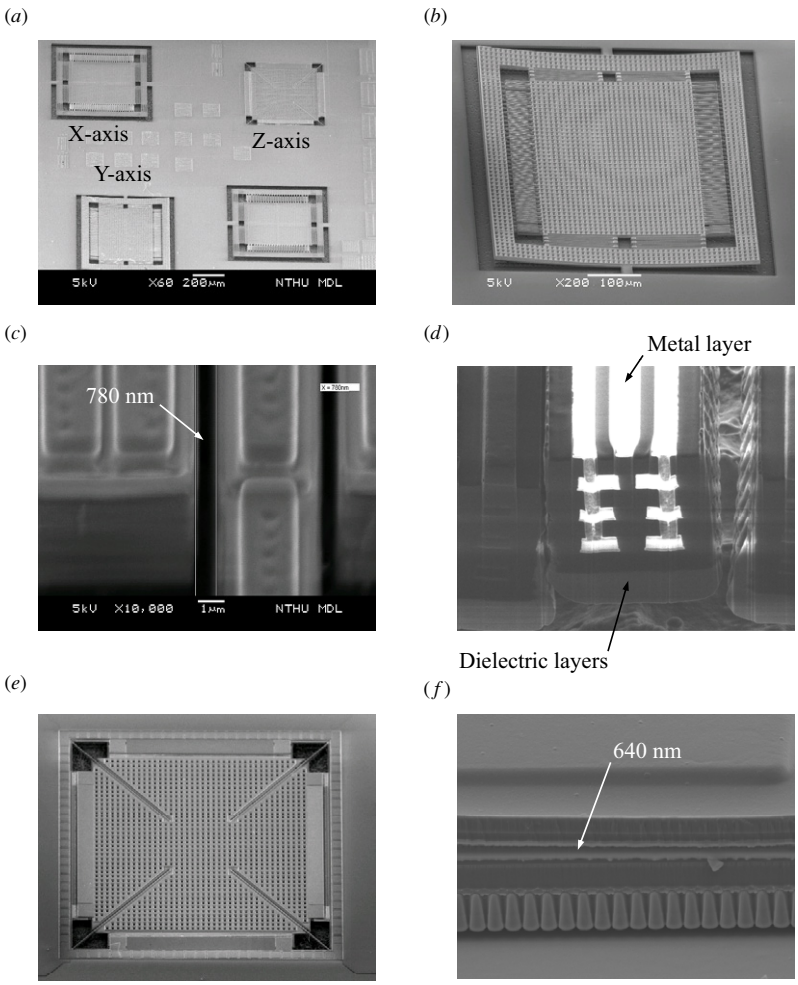

Figure 6. The SEM micrographs of (*a*) the fabricated chip containing the three-axis CMOS-MEMS accelerometers, (*b*) the in-plane accelerometer, (*c*) the zoom-in of the 780 nm in-plane sensing gap, (*d*) the cross section of the in-plane sensing electrodes, (*e*) the out-of-plane accelerometer and (*f*) the zoom-in of the 640 nm out-of-plane sensing gap.

dark region shows the dielectric layer used to protect the sensing electrodes. The SEM micrograph in figure 6(*e*) shows the *Z*-axis accelerometer. A pair of the out-of-plane sensing electrodes is highlighted by the zoom-in micrograph in figure 6(*f*). The sub-micron gap defined by the thickness of the M3 metal layer was 640 nm. Moreover, the large area plate-type sensing electrodes implemented by the present process are also demonstrated. As indicated in figure 2, the chip fabricated using the present process is mainly covered with the silicon dioxide film which is transparent under optical microscopy. In other words, the monolithically integrated sensing circuits and the routing wires underneath the transparent silicon dioxide films can still be clearly observed under the optical microscope, as demonstrated in figure 7.

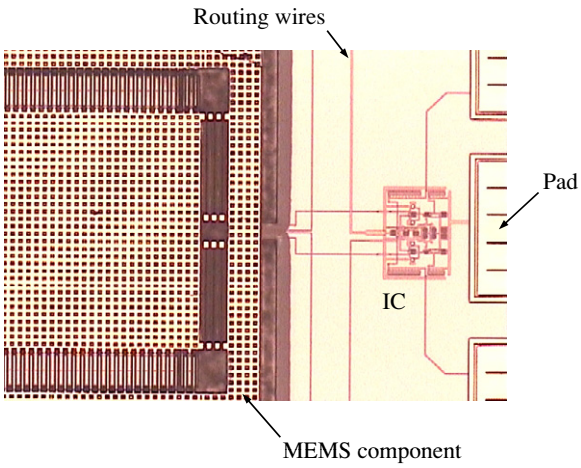

Figure 7. Photo of the CMOS chip to show the mechanical structure and sensing circuit. The sensing circuit covered by the transparent dielectric films is clearly observed.

3.2. Testing results

The fabricated CMOS-MEMS sensing chip was packaged inside a ceramic housing and connected to a printed circuit board (PCB) for future performance testing, as shown in figure 8(*a*). The experimental setup in figure 8(*b*) was established to test and calibrate the performance of the three-axis accelerometers. The PCB containing the sensor chip was mounted on the shaker. The vibration amplitude of the shaker was monitored by a commercial accelerometer during the test. Two anti-phase sinusoidal waves (1 V_{p-p} at 1 MHz) were input to modulate the capacitance change due to the driving

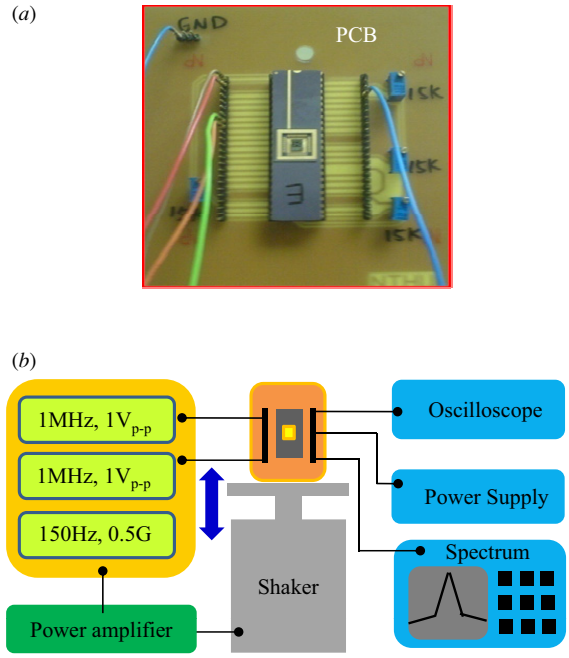

Figure 8. (*a*) The test unit containing a packaged CMOS chip mounted on the PCB, and (*b*) the measurement setup.

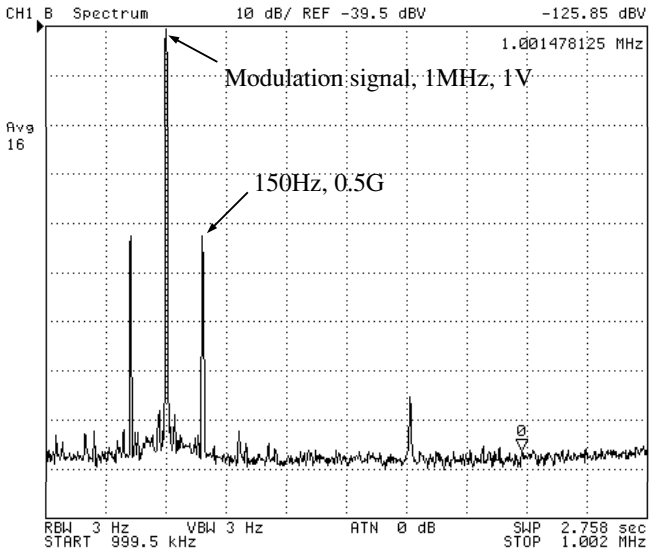

Figure 9. Typical spectrum results of an accelerometer at an excitation of 150 Hz, 0.5 G by using the shaker.

acceleration, and the sensing circuit worked under 5 V dc. The output signal from the fabricated accelerometers was displayed and recorded by a spectrum analyzer. Figure 9 shows typical results measured by a spectrum analyzer under 0.5 G excitation at 150 Hz. Figure 10 shows the variation of the measured output signal from the accelerometer with the input excitation by shaker. As shown in figure 10(*a*), the sensitivities for in-plane and out-of-plane accelerometers are respectively 11.5 mV G^{-1} and 7.8 mV G^{-1} within the measurement range

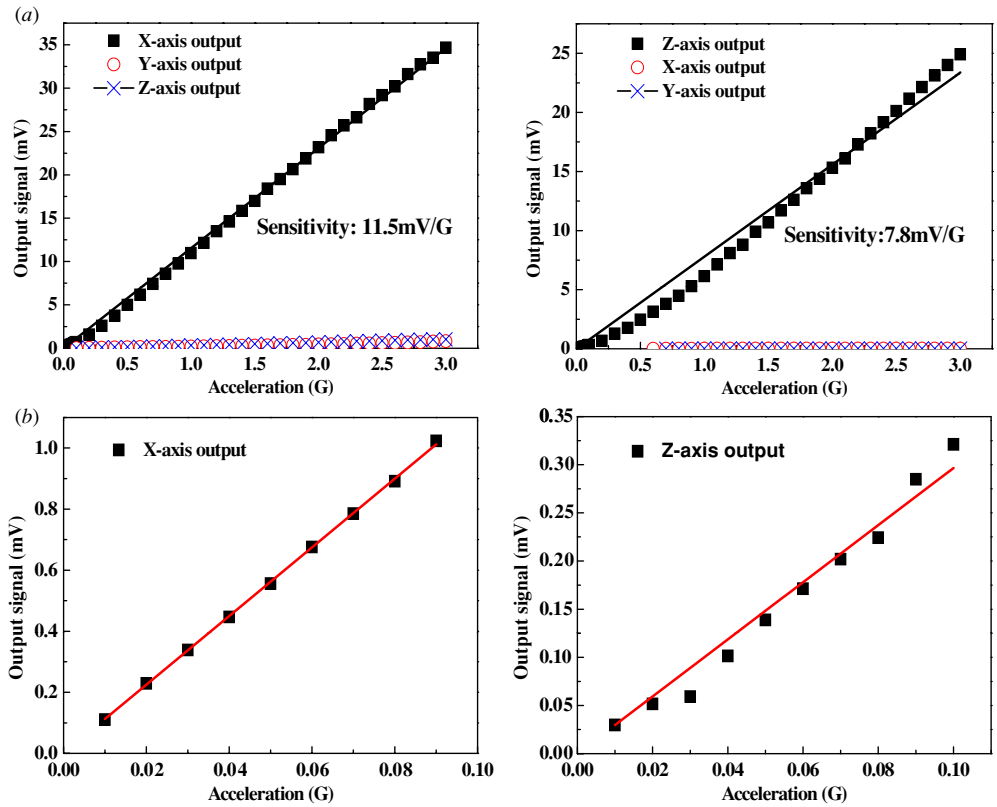

Figure 10. The variation of the measured output voltage with the input acceleration: (*a*) the acceleration range from 0.01 G to 3 G with an increment of 0.1 G, and (*b*) the acceleration range from 0.01 G to 0.1 G with an increment of 0.01 G.

of 0.01 G to 3 G. In addition, the nonlinearities for in-plane and out-of-plane accelerometers are respectively 0.5% and 3.7% within the full measurement range. As compared with the existing CMOS-MEMS accelerometers fabricated using the dry-etching approach [1, 2, 7, 8], the sensitivity is improved more than one order. The nonlinearity of the out-of-plane accelerometer is caused by the curling of the sensing plate. Figure 10(*b*) further shows the measured signal within the measurement range of 0.01 G to 0.1 G with an increment of only 0.01 G. The nonlinearities for in-plane and out-of-plane accelerometers respectively become 1.8% and 5.0% within such a measurement range. Moreover, according to the measured spectra, the noise floors are 2.4 mG $Hz^{-1/2}$ (in-plane accelerometer) and 4.1 mG $Hz^{-1/2}$ (out-of-plane accelerometer) with a modulation voltage of 1 V at 1 MHz. Table 1 summarizes the characteristics measured from the presented three-axis accelerometers CMOS chip, and also the comparison with the existing CMOS-MEMS accelerometers. Data in the last two columns are from this work.

4. Conclusion

This study presents a design to improve the performance of CMOS-MEMS gap-closing capacitive sensors. In addition to the standard CMOS process, the metal wet-etching approach is employed as the post-CMOS process to realize the present design. The MEMS structures are mainly made of the dielectric films of the CMOS process. Moreover, the metal layers and tungsten vias of the CMOS process are exploited as the sensing electrode and sacrificial layers. To demonstrate the feasibility of the present design, a CMOS-MEMS three-axis accelerometer chip is fabricated and characterized. Measurements show that the sensitivities of the accelerometer are 11.5 mV G^{-1} (in-plane accelerometer) and 7.8 mV G^{-1} (out-of-plane accelerometer), which are nearly one order of magnitude larger than the existing designs. Moreover, the excitation of 0.01 G is also detectable for both in-plane and out-of-plane accelerometers, and the nonlinearities become 1.8% (in-plane) and 5.0% (out-of-plane). In conclusion, there are two advantages of the presented approach for the CMOS-MEMS gap-closing capacitive sensor: (1) the dielectric MEMS structure successfully reduces the parasitic capacitance, and (2) sub-micron sensing gap and large area sensing electrode are realized by the wet etching of sacrificial metal layers to increase the performance of CMOS-MEMS capacitive sensors.

Acknowledgments

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