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# Implementation of a gap-closing differential capacitive sensing *Z*-axis accelerometer on an SOI wafer

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**Abstract**
This study presents a novel capacitive-type *Z*-axis (out-of-plane) accelerometer implemented on an SOI wafer. This accelerometer contains special designed gap-closing differential sensing electrodes. The present *Z*-axis accelerometer has four merits: (1) mass of the proof mass is increased by combining both device and handle silicon layers of the SOI wafer, (2) the sensitivity is improved by the gap-closing differential electrodes design, (3) the electrical interconnection between the device and handle silicon layers of the SOI wafer is available by means of the metal-vias, and (4) the sensing gap thickness is precisely defined by the buried-oxide layer of the SOI wafer. In application, the *Z*-axis accelerometer is fabricated and characterized. Typical measurement results demonstrate that the presented *Z*-axis accelerometer has a sensitivity of 196.3 mV $G^{-1}$ (42.5 fF $G^{-1}$) and a maximum nonlinearity of 2% over the range of 0.1–1 G.

(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

The MEMS accelerometer has been extensively applied to the automobile industry such as in electronic stability control (ESC), adaptive cruise control (ACC), air bag systems and crash detection. The MEMS accelerometer even finds more applications in consumer electronics, for instance, the cell phone, personal digital assistant (PDA), digital still camera (DSC) and video games. Thus, the requirement of a single-axis as well as a multi-axis accelerometer is rapidly increasing. Presently, various capacitive sensing approaches, such as the gap-closing electrodes [1–3], vertical comb electrodes [4–6], etc, have been employed for inertial sensors. Differential capacitive sensing is a promising approach to provide a larger signal, higher common-mode rejection ratio, larger voltage swing and higher linearity [7]. To date, many capacitive sensing accelerometers have been realized using different micro-fabrication technologies, for instance, surface micromachining [1, 2], bulk micromachining [6], integration of surface and bulk micromachining [8], and the CMOS–MEMS process [3–5, 9]. Moreover, these approaches have been further employed to demonstrate the monolithic integration of a three-axes accelerometer [5, 10].

Fabrication of MEMS devices using an SOI (silicon-on-insulator) wafer has various advantages, for instance, the superior material properties of a single crystal material, thick device is easily achieved, has less residual stresses, has simple fabrication processes, etc. Thus, the implementation of inertial sensors using an SOI wafer has gradually been increased [11–17]. Nevertheless, it remains a challenge to realize the *Z*-axis accelerometer and further monolithically integrate the three-axes accelerometer into the SOI wafer. In [11], the three-axes capacitive accelerometer, fabricated on an SOI wafer, has been successfully demonstrated. However, differential capacitive sensing is not available in the *Z*-axis direction. The vertical comb electrode has been employed in [12] to realize a *Z*-axis accelerometer with differential capacitive sensing, and has been further extended to implement a three-axes accelerometer on the SOI wafer [13].

In this study, the development of a novel SOI *Z*-axis accelerometer is reported. Both the device and handle silicon layers are exploited to fabricate the capacitive sensing

 

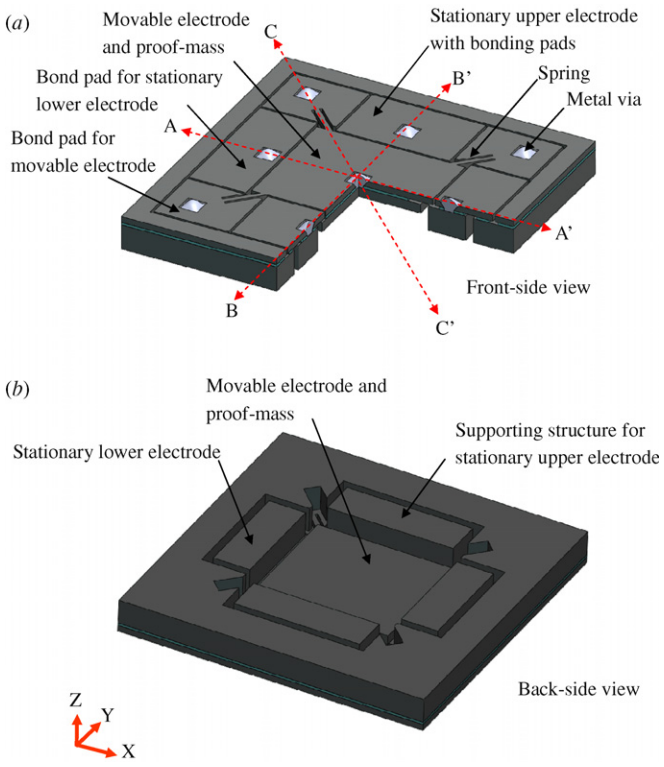


**Figure 1.** The schematic illustrations of the present *Z*-axis SOI accelerometer showing (*a*) the front-side view of the accelerometer formed by the device Si layer of the SOI wafer, the springs, proof mass and movable electrodes, bonding pads and stationary electrodes, and metal-vias, are clearly observed; and (*b*) the backside view of the accelerometer formed by the handle Si layer of an SOI wafer.

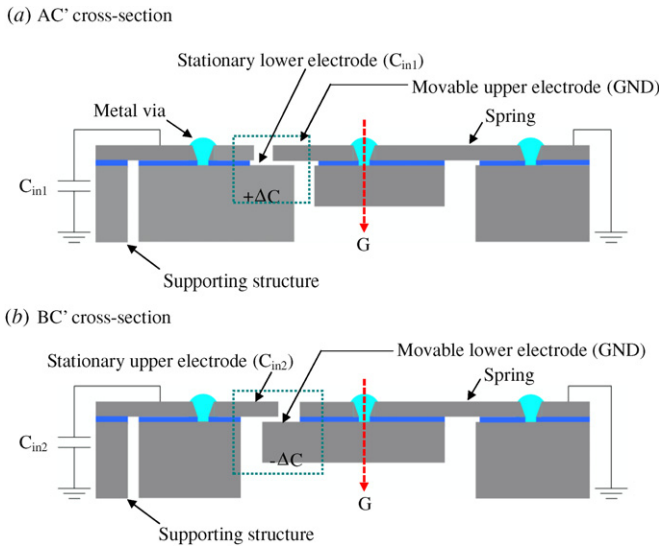


**Figure 2.** The schematic illustrations of the AC' and BC' cross sections indicated in figure 1 showing (*a*) the sensing electrodes in the AC' cross section containing a movable upper electrode (device Si layer) on proof mass and a stationary lower electrode (handle Si layer), where the signal on the stationary lower electrode is transmitted to the bonding pad (made of the device Si layer) by means of the metal-via; and (*b*) the sensing electrodes in the BC' cross section containing a movable lower electrode (handle Si layer) and a stationary upper electrode (device Si layer), where the stationary upper electrode is supported by the handle Si layer underneath.

electrodes. Thus, the gap-closing differential sensing electrodes are successfully demonstrated in the present SOI *Z*-axis accelerometer. The buried-oxide layer thickness of the SOI wafer is used to define the sensing gap. Metal-vias are used to establish electrical interconnection between the device and the handle silicon layers. Thus, the signal detected by the electrode, made up of the handle silicon layer, can easily be transmitted through the metal-vias. The present *Z*-axis accelerometer has the potential to enable the monolithic integration of the existing in-plane accelerometers to realize the three-axes SOI accelerometer.

## 2. Design concept

This study presents the design of a gap-closing differential capacitive sensing *Z*-axis accelerometer on an SOI wafer. The schematic illustration in figure 1(*a*) shows the front-side view of the accelerometer formed by the device silicon layer of an SOI wafer. In addition, figure 1(*b*) shows the backside view of the accelerometer formed by the handle silicon layer of an SOI wafer. The accelerometer consists of four springs, one proof mass, four pairs of gap-closing sensing electrodes (each pair of gap-closing sensing electrodes contains one movable electrode and one stationary electrode) and several metal-vias as the electrical interconnections for the device and handle silicon layers. The movable electrodes are on the proof mass, whereas the stationary electrodes are fixed to the substrate. As indicated in figure 1(*a*), the device silicon layer of the accelerometer is partitioned into five electrical isolated regions by trenches. For instance, the central proof mass, together with the four springs and their anchors, is connected and can be regarded as one electrical isolated region. The two rectangular areas along the *BB*' axis, containing two stationary upper electrodes and their bonding pads, are regarded as another two electrical isolated regions. Finally, the last two electrical isolated regions are the two rectangular areas along the *AA*' axis, which act as the bonding pads for the stationary lower electrodes. The metal-vias are employed as the electrical interconnection to transfer the signal detected by the stationary lower electrodes (handle layer) to the upper bonding pads (device layer). As indicated in figure 1(*b*), there are four mesas formed by the handle Si layer. Two of these mesas act as the supporting structures for the stationary upper electrodes, and the other two mesas are used as the stationary lower electrodes.

Figure 2 further shows the schematic illustrations of the AC' and BC' cross sections indicated in figure 1. As depicted in figure 2(*a*), the pair of sensing electrodes, as shown in the AC' cross section, contain a movable upper electrode on proof mass (formed by the device silicon layer) and a stationary lower electrode (formed by the handle silicon layer). On the other hand, as indicated in figure 2(*b*), the pair of sensing electrodes, shown in the BC' cross section, contain a movable lower electrode (still on proof mass but formed by the handle silicon layer) and a stationary upper electrode (formed by the device silicon layer). As the proof mass is subjected to an acceleration in the downward direction, the movable electrodes

**Table 1.** The detailed specifications of a typical accelerometer design.

| The detailed specifications of a typical accelerometer design | |
|---|---|
| Chip size | 5 mm × 5 mm |
| Mass | 0.4 $\mu$g |
| Spring constant | 36.6 N m$^{-1}$ |
| Sensing gap | 2 $\mu$m |
| Initial sense capacitance | 442 fF |
| Sensitivity | 48 fF G$^{-1}$ |

for both AC' and BC' cross sections will have a downward displacement. Thus, the sensing electrodes indicated in the AC' cross section will experience a decrease in the sensing gap, and this will result in a capacitance change of $+\Delta C$. Meanwhile, the sensing electrodes, as indicated in the BC' cross section, will experience an increase in the sensing gap and lead to a capacitance change of $-\Delta C$. As a result, such a design forms differential type capacitive sensing electrodes to improve the sensitivity and the signal-to-noise ratio. Since the metal-vias are employed as the electrical interconnection between the device silicon layer and handling silicon layer, the parasitic capacitance between these two layers is reduced.

A typical accelerometer was designed in this study to demonstrate the feasibility of the present approach. A sensitivity of approximately 50 fF G$^{-1}$ was selected as the design specification for the accelerometer. In addition, the accelerometer was designed to have a resonant frequency of near 3 kHz. The SOI wafer used in this study had a device layer of 18 $\mu$m thick, so that the spring stiffness was tuned to be 36.6 N m$^{-1}$ by varying its length and width. Moreover, the mass of the proof mass was tuned to be 0.4 $\mu$g by varying its length, width and thickness. Thus, the resonant frequency of the typical accelerometer design was 3.05 kHz. According to the overlap area and the 2 $\mu$m gap (determined by the oxide layer thickness of the SOI wafer) between the sensing electrodes, the accelerometer had an initial sense capacitance of 442 fF. As a result, the sensitivity of the accelerometer design was 48 fF G$^{-1}$. The specifications of the typical accelerometer design are summarized in table 1.

In summary, the present *Z*-axis accelerometer has four merits: (1) the sensitivity of the accelerometer is improved since the mass of the proof mass is increased by containing both device and handle silicon layers, (2) the sensitivity is also improved by the gap-closing differential capacitive sensing electrodes design, (3) the electrical interconnection between the device and handle silicon layers of the SOI wafer is available by means of the metal-vias, thus the parasitic capacitance is reduced and the electrical routing from the handle layer to the device layer becomes easier, and (4) the sensing gap thickness is precisely defined by the buried oxide of the SOI wafer.

## 3. The fabrication process and results

The fabrication process steps are illustrated in figure 3. In addition, table 2 summarizes the specifications of the SOI wafer employed in the process. As shown in figure 3(*a*), the processes began with the growth of 1 $\mu$m thick thermal oxide on the SOI wafer, and then the first photo mask was used to pattern the in-plane shape of the accelerometer on the device silicon layer. After that, the 100 nm $Si_xN_y$ film was deposited using low pressure chemical vapor deposition (LPCVD) and then patterned by the second photo mask. The LPCVD–$Si_xN_y$ film was used to define the metal connection window during the following bulk silicon etching. As shown in figure 3(*b*), the SOI wafer was immersed into KOH solution for anisotropic silicon etching. This bulk micromachined cavity acted as the via hole between the device silicon layer and the handle silicon layer. In addition, a 1 $\mu$m thermal oxide was grown to protect the surface of the bulk micromachined cavity. After that, both the front-side and backside LPCVD–$Si_xN_y$ films were removed by reactive ion etching (RIE). As shown in figure 3(*c*), the third mask was used to pattern the oxide on the handle layer (backside of the SOI wafer) to define the dimensions of the proof mass and sensing electrodes. Moreover, a photoresist was deposited on the backside of the SOI wafer and then patterned by the fourth mask. Thus, the surface of the handle layer at the backside of the SOI wafer was covered with patterned thermal oxide and photoresist layers. This approach enabled the fabrication of proof mass and sensing electrodes on the handle silicon layer. As shown in figure 3(*d*), the first deep reactive ion etching (DRIE) was used to define the thickness $h$ of the proof mass and movable lower electrode. The substrate was then immersed into buffer oxide etch (BOE) solution to remove the oxide layer which was not protected by the photoresist. As shown in figure 3(*e*), the second DRIE was used to etch through the handle silicon layer. The DRIE etching was stopped as the buried-oxide layer was first exposed. Thus, the handle silicon layer of thickness $h$ remaining on the SOI wafer acted as the proof mass and movable lower sensing electrode. In addition, a front-side DRIE was employed to define the in-plane shape of the accelerometer, including the proof mass, upper sensing electrode and springs on the device layer. As shown in figure 3(*f*), the etching mask and sacrificial layers were then removed using HF solution, and the accelerometer was released from the substrate. Finally, the silver paste was dispensed in the bulk micromachined cavity (via hole) for the electrical interconnection between the device and handle silicon layers.

**Table 2.** The specifications of the SOI wafer used in the process.

| The specifications of the SOI wafer | |
|---|---|
| Device layer thickness | 18 $\mu$m |
| Device layer resistivity | 0.001–0.004 ohm cm |
| Handle layer thickness | 400 $\mu$m |
| Handle layer resistivity | 0.001–0.004 ohm cm |
| Buried-oxide thickness | 2 $\mu$m |

In application, the proposed *Z*-axis accelerometer design was implemented on the SOI wafer with an 18 $\mu$m thick device silicon layer. Figure 4 shows the scanning electron microscopy (SEM) micrographs of a typical fabricated accelerometer. The front-side view of the accelerometer in figure 4(*a*) shows the

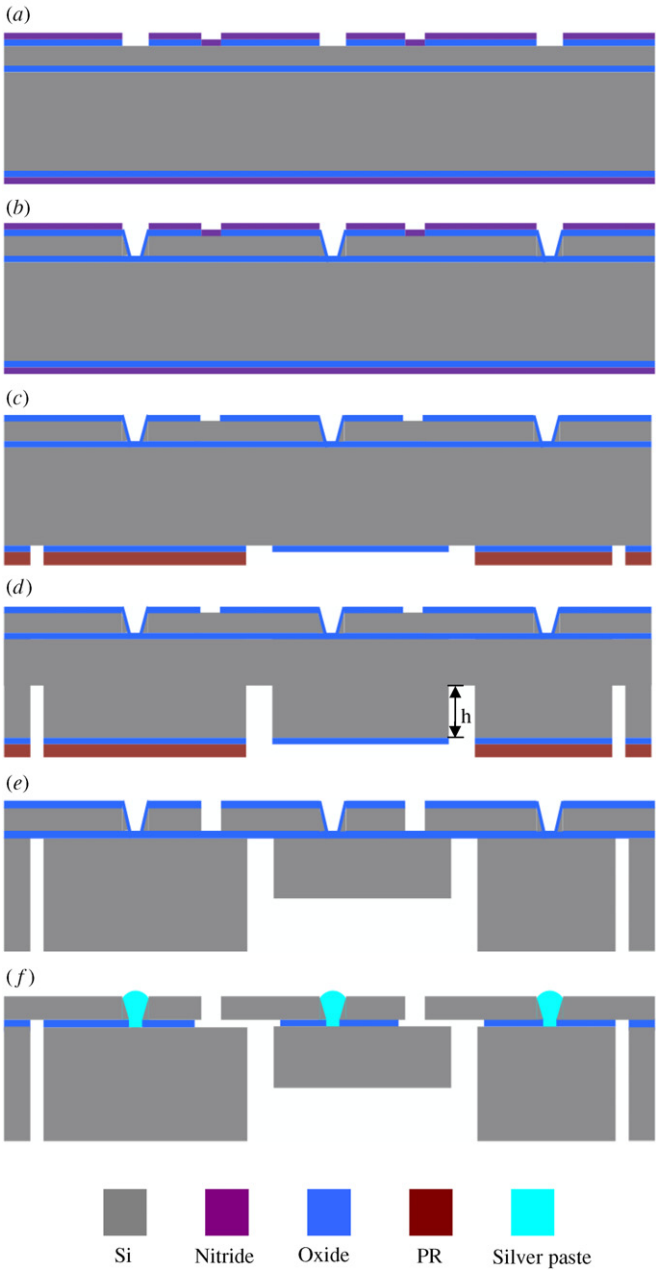


**Figure 3.** The fabrication process steps.

components made up of an 18 $\mu$m thick device Si layer. The components of the accelerometer, such as the spring, proof mass, upper sensing electrodes and via holes (before the silver dispensing) are clearly observed. The backside view of the accelerometer in figure 4(*b*) shows the components made of the handle Si layer. The central proof mass of thickness, as defined in figure 3(*d*), is clearly observed, and the four surrounded mesas are partitioned by the trenches after the DRIE in figure 3(*e*). Two of these mesas were used as the lower electrodes, and the other two mesas were used as the supporting structures for the upper electrodes. The zoom-in SEM micrograph in figure 5(*a*) shows the differential sensing electrode consisting of movable (on proof mass) and stationary electrodes (on substrate). In addition, the device and handle silicon layers on the proof mass, respectively,

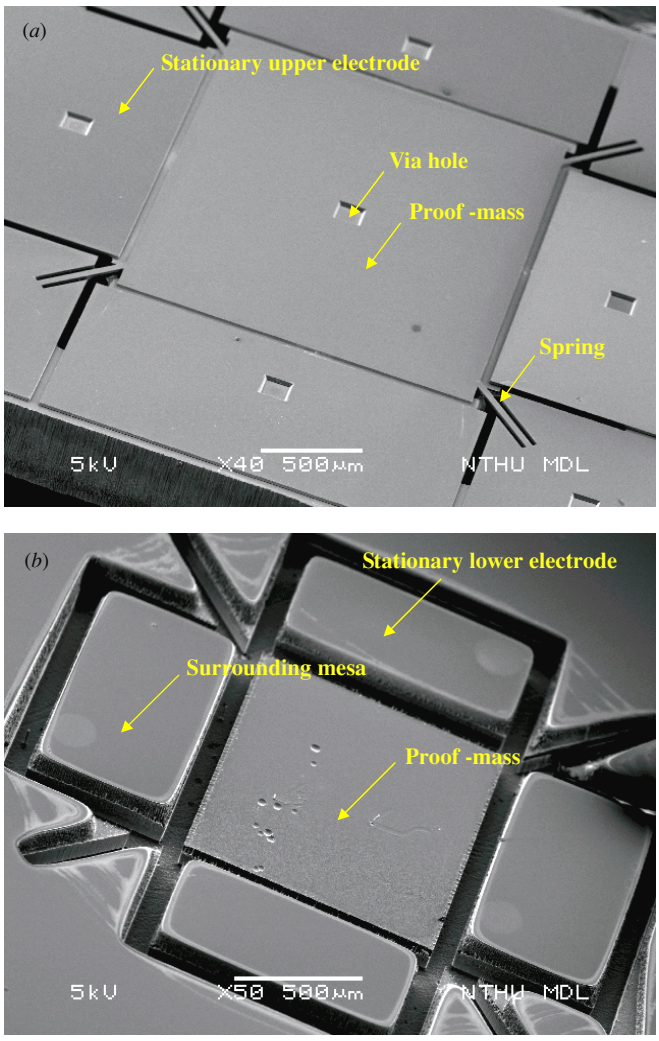


**Figure 4.** The SEM micrographs of a typical fabricated accelerometer where (*a*) the front-side view shows the components made of the device Si layer, and (*b*) the backside view shows the components made of the handle Si layer.

formed the movable upper and lower electrodes, as indicated in this micrograph. The zoom-in micrograph in figure 5(*b*) further shows the 2 $\mu$m sensing gap between the movable electrode (lower electrode) and the stationary electrode (upper electrode). The sensing gap thickness is precisely defined by the buried-oxide layer in the SOI wafer.

## 4. Testing and results

This study also characterized the performance of the fabricated accelerometer. Before testing, the via hole of the fabricated accelerometer in figure 4(*a*) was filled with silver paste by using the commercial pneumatic dispensing system. Thus, the electrical interconnection between the device layer and the handle layer was implemented. After that, the accelerometer was wire bonded and packaged in a ceramic house. As a result, the photo in figure 6(*a*) shows the chip after silver paste dispensing (for metal interconnect) and wire bonding. The photo in figure 6(*b*) shows the final packaged accelerometer in the ceramic housing.

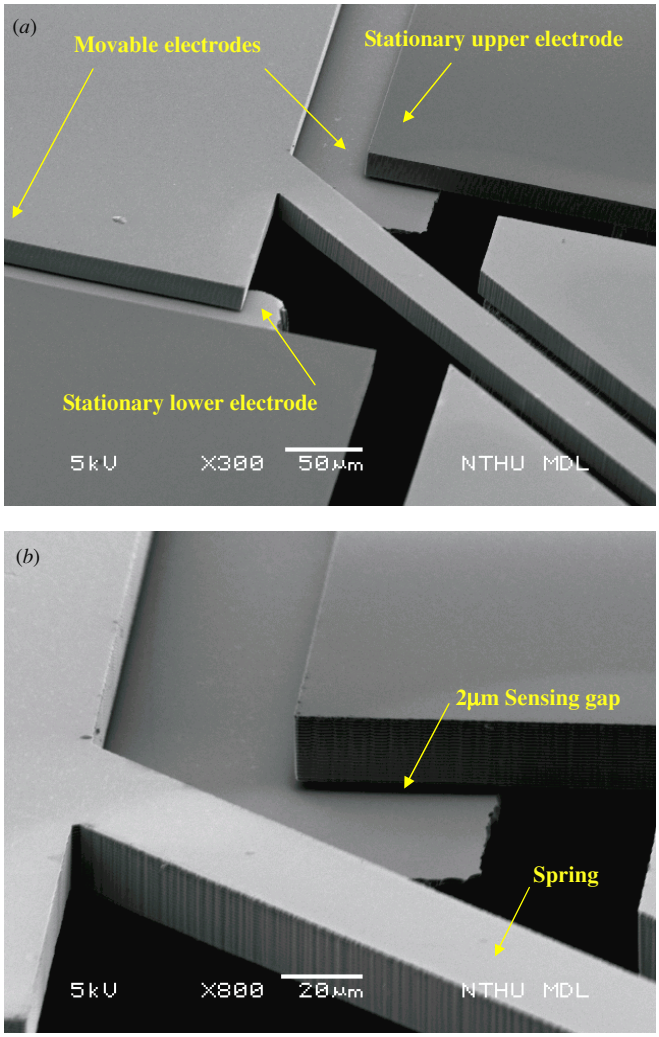


**Figure 5.** The zoom-in SEM micrographs show (*a*) the differential sensing electrodes, and (*b*) the gap between the movable and the stationary electrodes.

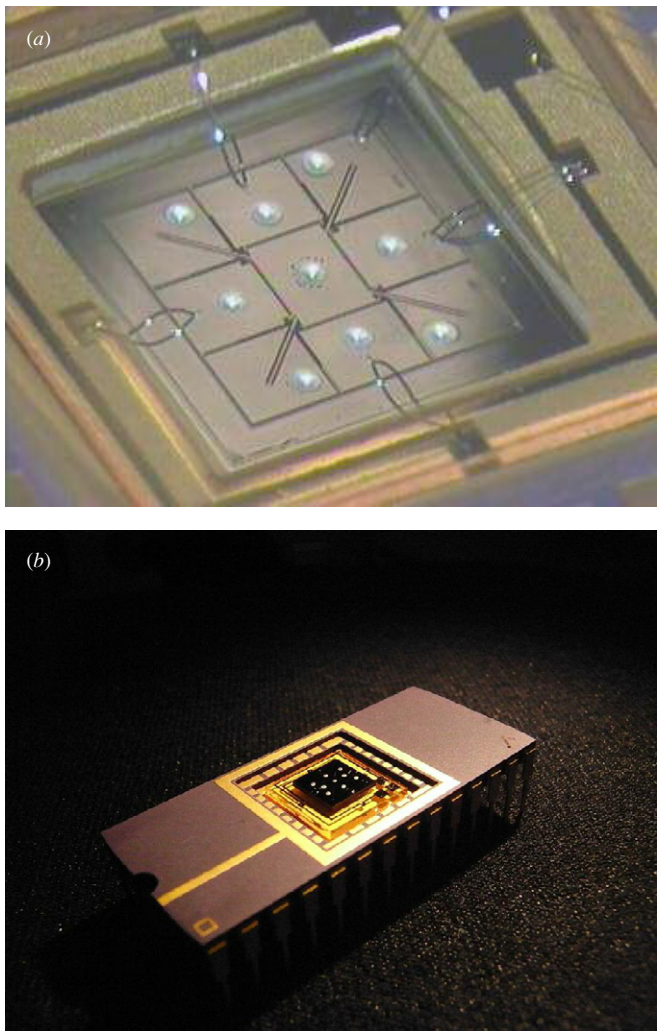


**Figure 6.** The photos show (*a*) the chip after silver paste dispensing and wire bonding, and (*b*) the final packaged accelerometer in the ceramic housing.

The measurement setup in figure 7 was used to characterize the performance of the *Z*-axis accelerometer [9]. A shaker (V40 B electrodynamic shaker, by LDS Group Inc., USA) and a function generator were used to provide a base motion to excite the packaged *Z*-axis accelerometer. The dynamic characteristic of the shaker was also monitored by using a commercial accelerometer. The capacitive signal detected by the present SOI accelerometer was converted into an output voltage by using a commercial capacitive readout IC (MS3110 Universal Capacitive Readout$^{TM}$ IC, by Irvine Sensors Corporation, USA) [18]. After that, the output voltage was displayed and recorded by the oscilloscope and the spectrum analyzer. Figure 8 shows the typical measured frequency response recorded by the spectrum analyzer as the accelerometer was driven by the shaker with 1 G harmonic (sinusoidal) excitation. The measurement results in figure 9(*a*) show the output voltages of the *Z*-axis accelerometer with the excitation ranging from 0.1 G to 1 G. In this measurement range, the sensitivity and nonlinearity of the present accelerometer are, respectively, 196.3 mV G$^{-1}$ (the measured capacitance, 42.5 fF G$^{-1}$, can be determined from the transfer function of MS3110 [18]) and 2%. In addition, the noise floor can be determined from [10]:

$$\text{Noise floor} = \frac{\text{output noise}}{\text{sensitivity}} \times \frac{1}{\sqrt{\text{bandwidth}}}, \qquad (1)$$

where the output noise and the bandwidth are measured by the Agilent 4395A network analyzer. Thus, the noise floor determined from equation (1) was 0.76 mG Hz$^{-1/2}$. Moreover, the accelerometer also experienced the in-plane excitations by the shaker to characterize its cross-axis sensitivities. As indicated in figure 9(*a*), the cross-axis sensitivities in the *X*-axis and the *Y*-axis are less than 1.94% and 1.32%, respectively. The measurement results in figure 9(*b*) further indicate that the minimum acceleration detected by this accelerometer can reach 0.01 G. However, according to the limitation of the shaker and function generator, the input acceleration value of less than 0.01G cannot be provided by the excitation system. Thus, the resolution of the present accelerometer was not characterized. The characteristics of the present accelerometer are summarized in table 3. Measurement results demonstrate

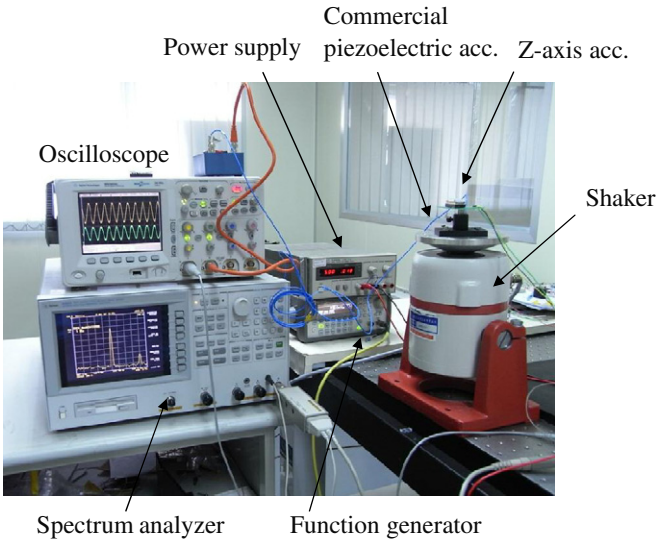


**Figure 7.** The measurement setup to characterize the performance of the accelerometer.

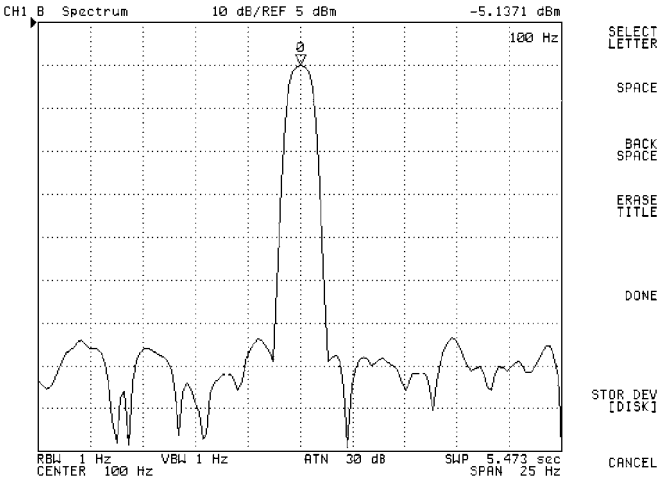


**Figure 8.** The typical measured frequency response recorded by the spectrum analyzer.

**Table 3.** The characteristics of the present *Z*-axis SOI accelerometer.

| The characteristics of the present *Z*-axis SOI accelerometer | |
|---|---|
| Measurement range | 1 G |
| Bandwidth | 100 Hz |
| Sensitivity | 42.5 fF $G^{-1}$ |
| Nonlinearity | 2% |
| Cross-axis sensitivity *X* | 1.94% |
| Cross-axis sensitivity *Y* | 1.32% |
| Noise floor | 0.76 mG $Hz^{-1/2}$ |

the feasibility of the present *Z*-axis accelerometer on an SOI wafer. In comparison with the existing *Z*-axis accelerometer fabricated on an SOI wafer, the sensitivity of the present case is higher than that of a vertical-comb design [13], as shown in table 4.

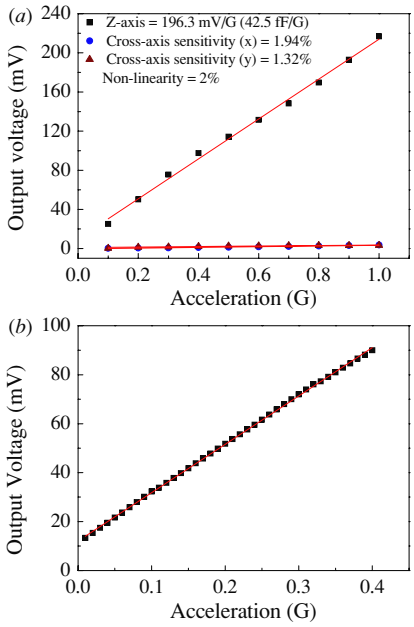


**Figure 9.** The typical measurement results of (*a*) the output voltage of the *Z*-axis accelerometer at different excitations and the cross-axis sensitivities at the measurement range of 0.1–1 G; and (*b*) the *Z*-axis accelerometer at the measurement range of 0.01–0.4 G with an increment of 0.01 G each time.

**Table 4.** Comparison of the present accelerometer with that reported in [13].

| | Reference [13] | Present device |
|---|---|---|
| Resonance frequency | 5.05 kHz | 3.05 kHz |
| Initial sense capacitance | 1 pF | 442 fF |
| Sensitivity | 1.1 fF $G^{-1}$ | 42.5 fF $G^{-1}$ |

## 5. Conclusions

The implementation of an inertial sensor on the SOI wafer is a promising approach. Presently, various capacitive-type accelerometers on SOI wafers have been reported. However, it remains a challenge to fabricate the capacitive-type *Z*-axis (out-of-plane) accelerometer on an SOI wafer. This study successfully implements a novel capacitive-type linear accelerometer on an SOI wafer to detect the motion in the out-of-plane direction. The accelerometer contains differential capacitive sensing electrodes with a gap closing design on an SOI wafer. The sensing gap thickness is precisely defined by the buried oxide layer. The metal-vias are used as the electrical interconnect for the lower electrode (on the handle silicon layer). The measurement results demonstrate that the present *Z*-axis accelerometer has a sensitivity of 196.3 mV $G^{-1}$ (42.5 fF $G^{-1}$) and a maximum nonlinearity of 2% over the range of 0.1–1 G. The cross-axis sensitivities of the accelerometer are less than 1.94% (in the *X*-axis) and 1.32% (in the *Y*-axis) over the same measurement range.

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