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Implementation of three-dimensional SOI-MEMS wafer-level packaging using through-wafer interconnections

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Abstract
Packaging is an emerging technology for microsystem integration. The silicon-on-insulator (SOI) wafer has been extensively employed for micromachined devices for its reliable fabrication steps and robust structures. This research reports a packaging approach for silicon-on-insulator-micro-electro-mechanical system (SOI-MEMS) devices using through-wafer vias and anodic bonding technologies. Through-wafer vias are embedded inside the SOI wafers, and are realized using laser drilling and electroplating. These vias provide electrical signal paths to the MEMS device, while isolating MEMS devices from the outer environment. A high-strength hermetic sealing is then achieved after anodic bonding of the through-wafer-vias-embedded SOI wafer to a Pyrex 7740 glass. Moreover, the packaged SOI-MEMS chip is compatible with surface mount technology, and provides a superior way for 3D heterogeneous integration.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

MEMS packaging, unlike its IC counterpart, is not only a useful approach to protect fragile micromachined devices but also an emerging technology for the integration of microsystems. MEMS packaging is still a challenge since micro devices typically consist of complicated three-dimensional structures and moving components. In addition, special packaging requirements may also be needed for different applications of MEMS devices. For instance, a transparent cover is required for some of the optical devices to allow the input and output of light [1, 2]. A low pressure ambient is required for some of the inertia sensors, such as vibrating gyros [3], to increase its quality factor and sensitivity. In this regard, hermetic sealing is a key issue for MEMS packaging. However, the electrical interconnect between the MEMS device and the bonding pad becomes a critical problem for hermetic sealing [4]. Various wafer-bonding techniques have been reported to achieve hermetic sealing of a non-planarized MEMS surface [1, 5, 6].

Presently, the SOI (silicon-on-insulator) substrate has been extensively employed in MEMS devices because of its simple yet reliable fabrication steps, higher yield and robust structures. Various transducers such as accelerometers, optical switches, etc, have been successfully demonstrated using SOI micromachining [7, 8]. Many SOI packaging processes are taking advantage of the rapidly growing technology of the through-wafer via. In these cases [9–11], through-glass vias deposited with a metal film are fabricated onto a Pyrex glass to act as the electrical interconnections. The SOI substrate with MEMS devices is encapsulated using these Pyrex 7740 with through-glass interconnections allowing hermetic sealing of SOI-MEMS devices to be achieved. Moreover, this through-silicon via (TSV) approach enables the 3D stacking of MEMS

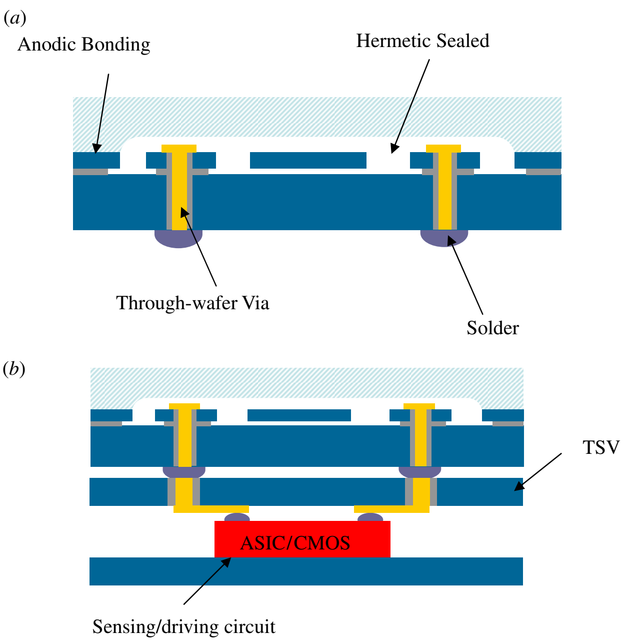

Figure 1. The present packaging model for SOI-MEMS wafer-level hermetic packaging.

and IC components [12, 13] realizing the miniaturization, and the heterogeneous integration of microsystems can be realized.

This research presents a wafer-level packaging of a SOI wafer with a Pyrex 7740 glass using the anodic bonding technique, as shown in figure 1(*a*). The fabrication process has been established to integrate the MEMS devices and through-wafer vias onto the SOI wafer. In addition, hermetic sealing is then achieved by bonding this processed SOI wafer to a Pyrex 7740 glass cap wafer. The present SOI wafer packaging technology is compatible with the surface mount technology (SMT). As shown in figure 1(*b*), this packaged device can further integrate with other heterogeneous chips using 3D stacking.

2. Concept and process steps

This study has established a process to implement the present packaging approach in figure 1(*a*). The process steps are illustrated in figure 2. The process began with a SOI wafer which had MEMS components patterned but not yet released onto the silicon layer of the device. As in figure 2(*a*), a 3 W UV-laser-drilled through-wafer via holes on the SOI substrate. Unlike DRIE (deep reactive ion etching), the UV laser can etch through both the silicon and the oxide layers on the SOI

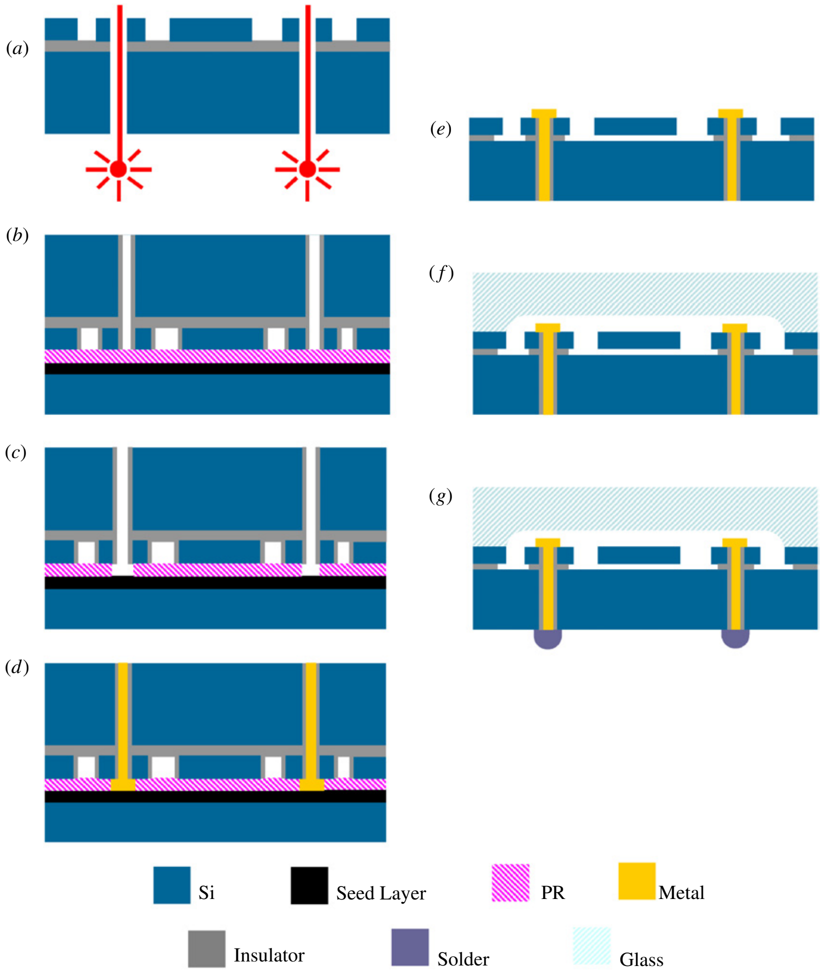

Figure 2. Process flow for SOI-MEMS wafer-level hermetic packaging.

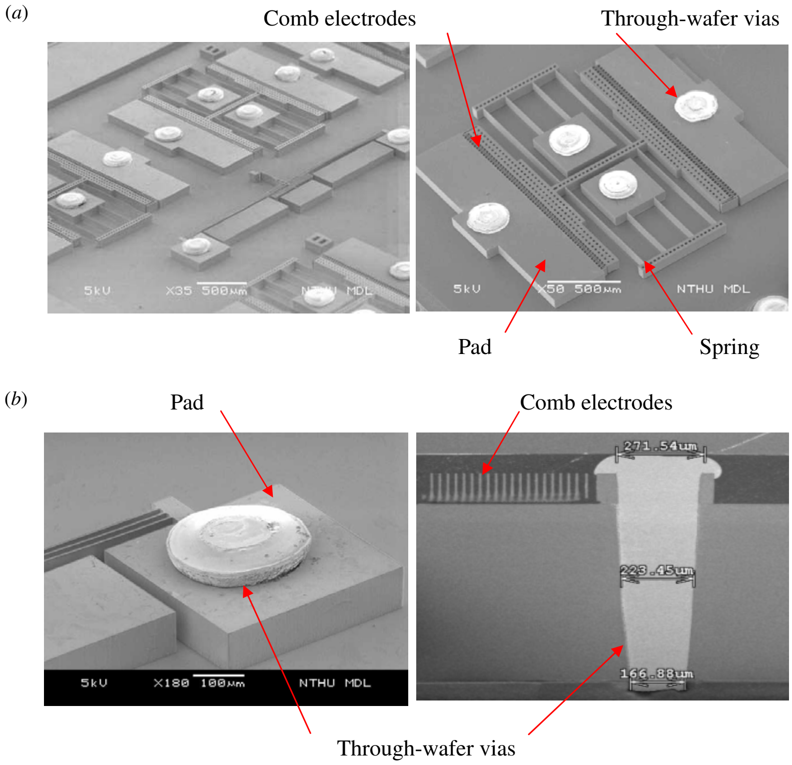

Figure 3. The fabrication results of through-wafer vias and SOI micromachined devices, (*a*) the SOI micro actuators with bond pads and through-wafer vias and (*b*) close-up and cross-sectional views of the through-wafer vias.

wafer. In general, an aspect ratio of 5 is available using this laser drilling technology. In this study, the diameter of holes ranged from 100 μm to 300 μm. Thus, photolithography on the patterned silicon device layer or on the backside of the SOI wafer was prevented. After that, a thermal oxide was grown and patterned so as to form an insulation layer on the sidewall of via holes. The device layer of the SOI wafer was glued to another auxiliary substrate by means of photoresist (PR), as shown in figure 2(*b*). A metal seed layer had already been deposited on this auxiliary substrate before spinning on photoresist. As shown in figure 2(*c*), the PR was patterned using the photolithography process. The SOI substrate acted as a conformal mask during PR exposure. The via holes were then filled using metal electroplating to form the via plug, as shown in figure 2(*d*) [14]. The electroplating process was initiated from the seed layer of the auxiliary substrate. A dc current of 300 mA was used during electroplating. This is a unique electroplating process which does not adopt a traditional seed layer on the via sidewall process, but uses a seed layer on the auxiliary substrate to avoid voiding caused by poor coverage on the sidewall. As shown in figure 2(*e*), after removing the auxiliary substrate in the stripper, the MEMS structures were released from the SOI substrate in the HF solution. As illustrated in figure 2(*f*), the SOI-MEMS devices were finally packaged after anodic bonding with the Pyrex glass. In this process, a voltage of 800 V and a temperature of 450 °C were adopted for anodic bonding. Finally, the solder was electroplated onto the backside of the SOI-MEMS packaged wafer to form the second level interconnection, as shown in figure 2(*g*). Thus, the packaged SOI-MEMS chip in figure 2(*g*) is SMT compatible. In conclusion, as shown in figure 1(*b*), the packaged SOI substrate with via-plug interconnections enables 3D heterogeneous integration.

3. Experiment and results

To demonstrate the feasibility of the present concept, micro actuators on the SOI wafer were fabricated and packaged using the processes in figure 2. In addition, various tests regarding the performance of packaging and device were also investigated.

3.1. Fabrication and integration

The SEM (scanning electron microscopy) photos in figure 3 show typical fabrication results of micro actuators and their integration with through-wafer vias on a SOI wafer. The left photo in figure 3(*a*) shows that various kinds of micro devices have been successfully fabricated using the present technology. No influence of the post-process packaging step was observed in the high yield SOI micromachining process. The right photo in figure 3(*a*) shows a comb-drive linear actuator which connects to the through-wafer via by means of the bonding pad. Figure 3(*b*) further shows the close-up and cross-sectional views of the through-wafer via. As shown in the left photo of figure 3(*b*), the mesa structure above the bonding pad is the electroplated via plug. The height of this mesa can be tuned by the thickness of the adhesive photoresist layer. Various step heights of the mesa, ranging from 10 to 40 μm, have been fabricated. The right photo of figure 3(*b*) shows the cross section of a via plug, and a suspended MEMS structure can also be observed. It clearly shows that no defects inside the

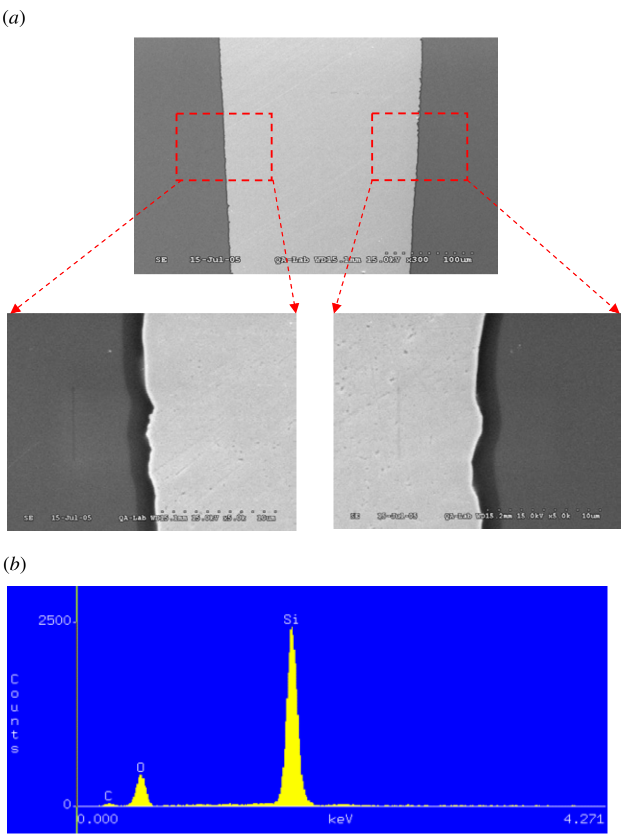

Figure 4. (*a*) Zoom-in view of the through-wafer vias and a nearby silicon substrate, and (*b*) the EDX analysis of the insulating material.

electroplating via plug are observed under this magnification. As indicated in this photo, the width of the UV-laser-drilled via plug ranges from 167 μm to 272 μm due to the energy distribution of the laser [15]. Thus, the diameter of the via hole is a design consideration for the present approach while using laser drilling. The zoom-in SEM photos in figure 4(*a*) show the conformal coverage of an insulation layer on the peripheral of a via hole. In addition, the electroplated metal of the via plug also conformally covers the surface of the insulation layer and completely fills up the via. The EDX (energy dispersive x-ray) analysis shown in figure 4(*b*) further demonstrates that the insulation layer between the metal and silicon is a SiO_2 film.

The photo in figure 5(*a*) shows the SOI-MEMS devices packaged with a Pyrex glass after anodic bonding, and the MEMS devices are seen through the transparent Pyrex glass. The SEM photo in figure 5(*b*) further shows the side view of the packaged SOI-MEMS chip which includes a glass cap, SOI substrate and a second level solder ball. This chip is ready to mount on a printed circuit board (PCB) using the SMT approach, as demonstrated in figure 6. The packaged SOI-MEMS chip with through-wafer vias has been mounted on top of the PCB board for assembly. The zoomed-in photos also show the SOI devices, such as the resonator and the linear accelerometer with through-wafer vias connecting to the bond pads on this chip. The device in figure 5 can also be employed for 3D heterogeneous integration, as shown in figure 1(*b*).

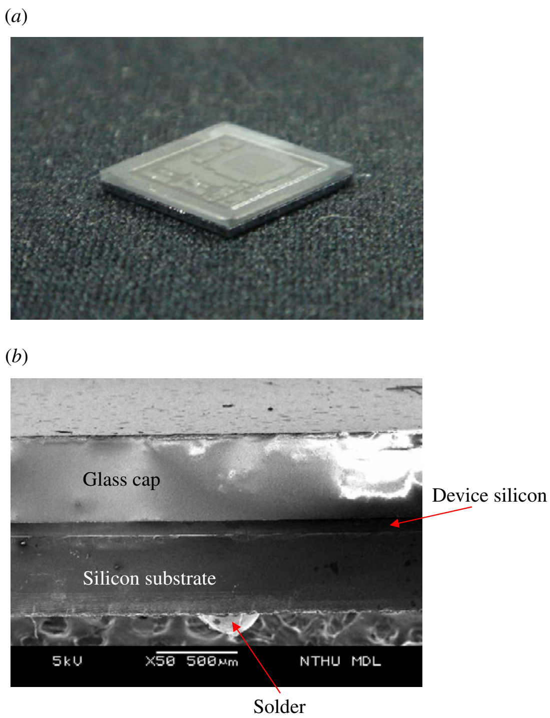

Figure 5. (*a*) Photo of a packaged SOI-MEMS chip covered by a Pyrex 7740 glass, and (*b*) the SEM photo of the side view of this packaged chip.

3.2. Tests

This study established the experimental setup in figure 7 to test the hermetic characteristic of the via plug prepared by the present packaging technology. The experimental setup contains a vacuum chamber, a mechanical pump, a pressure gauge and a test specimen. This test intended to record the pressure variation of the vacuum chamber to evaluate the hermetic characteristic of the via plug. The test specimen was a silicon substrate bonded with a Pyrex 7740 glass. This silicon substrate contained two UV-laser-drilled via holes, and one of the via holes was filled with the electroplated metal to form the via plug while the other was used as the inlet of the vacuum path. The cross-sectional view of a typical test specimen is shown in the SEM photo of figure 7. In order to obtain a pressure-controlled environment, the testing chamber was connected to a mechanical pump. The test specimen was glued to the vacuum chamber using epoxy, as indicated in the illustration. A pressure gauge is connected to the vacuum chamber to record pressure variation during testing. The initial pressure applied to this chamber was -9.07 kPa during the test, and the duration of the test was more than 1100 h. Figure 8 shows the variation of chamber pressure (in kPa) with the testing time (h). It indicates that the pressure variation of the chamber was -8.56 kPa–-9.6 kPa after 1100 h of testing. The slight pressure variance during testing may come from epoxy leakage or ambient disturbance, such as temperature change.

The test setup in figure 9 was also established to demonstrate the performance of the micromachined devices after the present processes. The test specimen was a micro V-beam thermal actuator driven in the in-plane direction by

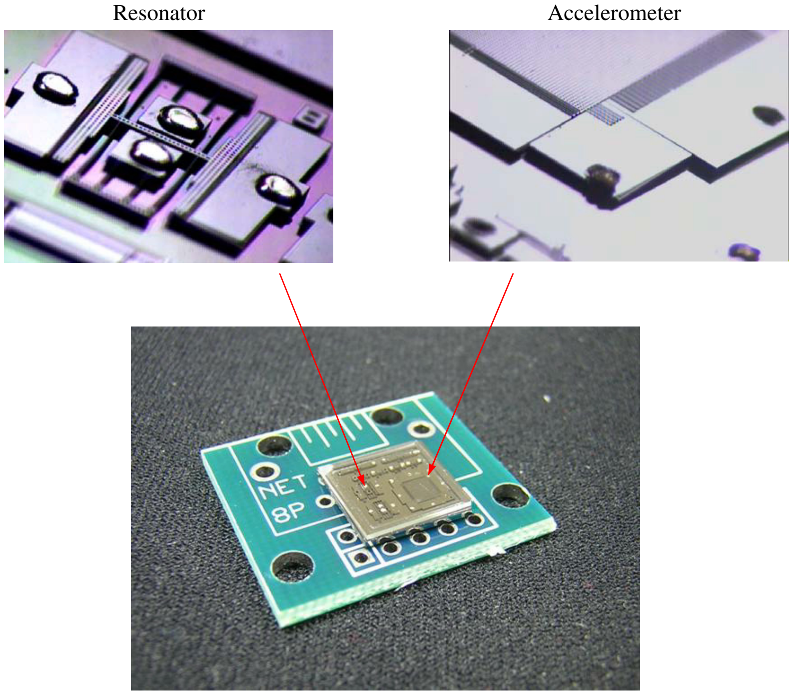

Figure 6. Photo of the packaged SOI-MEMS chip on top of a PCB, and the inset photos are the MEMS devices on the SOI wafer.

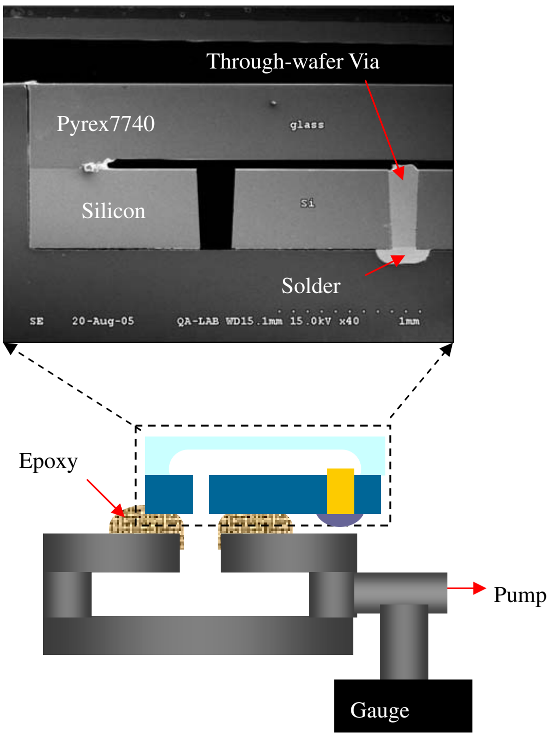

Figure 7. Experimental setup for hermetic testing.

a dc power supply [16]. The chip containing the thermal actuators was bonded on a PCB, and the driving signal from the power supply was input to the actuator through the via interconnects, as depicted in figure 9. The displacement of the actuator was measured using a commercial optical displacement detector with an in-plane resolution of 0.1 μm. Figure 10 shows the driving test results of the V-beam thermal

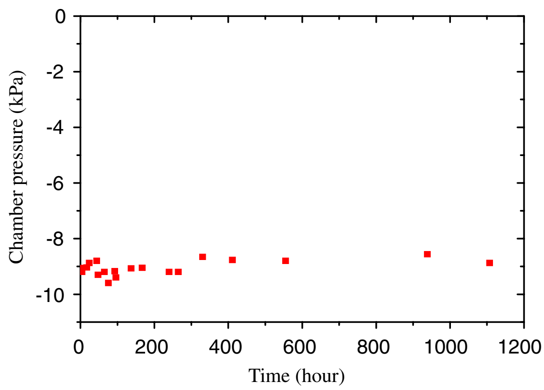

Figure 8. Measured variation of chamber pressure with the time period.

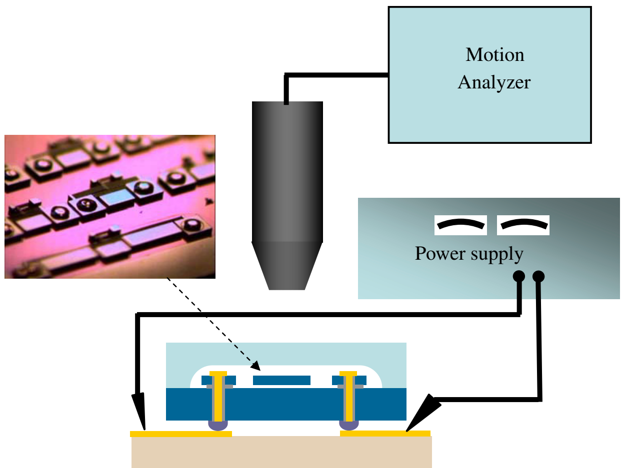

Figure 9. Experimental setup of the MEMS devices driving test; the driving voltage was input from the through-wafer vias.

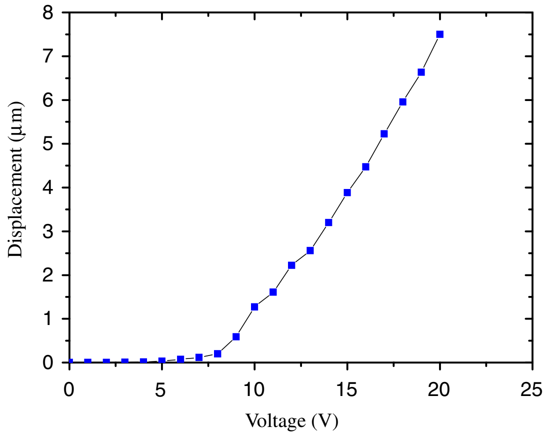

Figure 10. Measured variation of packaged thermal actuator displacements with the driving voltages.

actuator, and the pre-buckling and post-buckling deformations of the actuator are demonstrated. In short, the packaged device has been successfully driven through the vias.

4. Conclusions

This research demonstrates a novel packaging approach and fabrication process for SOI-MEMS devices. The present technique is achieved by means of through-wafer interconnections and anodic bonding. Through-wafer vias are embedded inside the SOI wafers using laser drilling and electroplating. These vias provide electrical signal paths to the MEMS device while isolating the device from the outer environment. In this study, the thermal oxide is conformally grown onto the surface of the via holes to act as the insulation layer between the silicon substrate and the via plug. A low-temperature conformal coating insulator film, such as parylene, could be a potential candidate for this insulation layer. Moreover, solder paste printing instead of electroplating can be used to form the second level interconnection in figure 2(*g*). Various tests have been conducted to evaluate the performances of the present packaging approach. The leakage test demonstrates the hermiticity of the packaged SOI-MEMS chip after anodic bonding. Driving of the thermal actuator shows that the signal can successfully input the packaged device through the vias. This packaging module is SMT compatible. Moreover, this approach can also be applied to implement through-wafer interconnects onto silicon substrates. Thus, a 3D heterogeneous integration of different chips, as illustrated in figure 1(*b*), can be achieved.

Acknowledgments

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