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Design and implementation of monolithically integrated sealed and unsealed chambers by using the wafer level packaging

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Abstract

This study presents the approaches to simultaneously realize various MEMS devices respectively encapsulated inside sealed and unsealed chambers by using the existing microfabrication and wafer level capping processes. In general, the wafer level capping process could encapsulate MEMS devices inside sealed chambers. In this study, the air leakage paths from the encapsulated chamber to the ambient have been selectively patterned and fabricated using the existing processes, so that the unsealed chambers are also achieved. The unsealed chamber is connected to the ambient and can be employed to encapsulate environmental monitoring devices such as humidity or pressure sensors. However, the sealed chamber is isolated with the ambient. The pressure in the sealed chamber is determined by the vacuum condition during the wafer level capping process. The sealed chamber could encapsulate devices such as motion sensors and resonators in the required vacuum condition. Thus, the presented approaches could enable existing process platforms to monolithically fabricate and encapsulate more devices for various applications. Devices such as micromachined Pirani gauge, resonator, and pressure sensor are fabricated and characterized to verify the present approaches. Measurement results indicate that sensors in different pressure conditions are respectively achieved by unsealed chambers and sealed chambers.

Keywords: unsealed chamber, leakage path, wafer level capping, MEMS

(Some figures may appear in colour only in the online journal)

1. Introduction

The emerging applications of micro-electromechanical systems (MEMS) in consumer electronics and artificial intelligence-internet of things (AI-IOT) drive the implementation of various sensors into lots of equipment for smartphones, smart cities, and machines networking [1]. Various MEMS sensors such as the accelerometer, gyroscope, magnetometer for motion detection, and the pressure sensor, humidity sensor, temperature sensor for environmental monitoring are incorporated into mobile devices. Thus, the fabrication processes for the mass production of MEMS sensors attract attention. Moreover, due to the numerous types of MEMS sensors that are awaiting to be integrated into consumer products, realizing combo sensors by either system in package (SiP) solution or system on chip (SoC) solution becomes more significant to fulfill compact, light, and multi-functions requirements. Presently, many commercially available MEMS platforms have been established by foundries, for example, the THELMA/Smeraldo technology by ST Microelectronics [2], the Silicon-above-CMOS (complementary metal-oxide semiconductor) by TSMC (Taiwan Semiconductor Manufacturing Company) [3], the MEMS platforms by X-FAB [4], the MIDIS platform by DALSA [5], the N&MEMS platform by

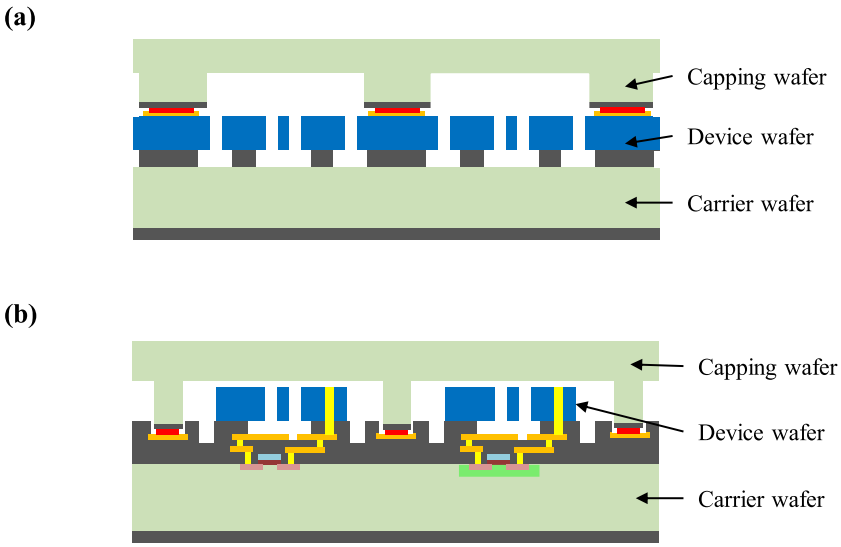
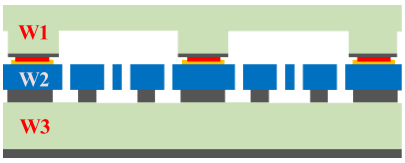
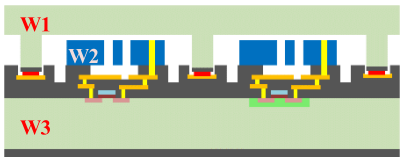


Figure 1. Silicon above CMOS foundry platforms, (a) the Bond on Device layer (BOD), and (b) the bond on carrier substrate scheme (BOC).

Table 1. Summary of the BOD and BOC fabrication platforms.

Platform	BOD	BOC
Process integration scheme		
Three wafers stacking by two bonding techniques	Silicon-oxide fusion bond first metal eutectic bond last	Silicon-oxide fusion bond first metal eutectic bond last
Three wafers functions	W1: capping w/i or w/o CMOS W2: MEMS functions W3: MEMS's carrier w/o CMOS	W1: capping W2: MEMS functions W3: MEMS's carrier w/i CMOS
Process sequences	Capping wafer (W1) and MEMS wafers (W2, W3) are processed separately and joined last	MEMS (W2) above CMOS (W3) wafer is processed. Capping wafer (W1) joined last
Reference	[18]	[3]

Tronics [6], and so on. The MEMS sensors of different functions can be fabricated and further monolithically integrated to achieve the SoC by using these process platforms. Moreover, the processes for combo sensors (SoC approach), especially for motion sensors and mechanical resonators, have also been demonstrated by fabless industries [7–9].

Most of the aforementioned fabrication platforms are equipped with the hermetic wafer level bonding process to protect the suspended MEMS structures from moisture and particles, and also to specify the pressure in the sealed chamber. In addition to the fabrication processes, the packaging related issues are also critical concerns to achieve commercial combo sensors (SoC approach). The MEMS sensors have diverse operating conditions and requirements. For instance, about inertia sensors, the vibratory-rate gyroscope is operating in a 0.1–1 Torr vacuum environment to sustain constant moving amplitude in the driving loop for stable angular rate tracking [10], whereas the linear accelerometer is operating in hundreds Torr ambient to offer air damping. Moreover, it is required for some MEMS sensors such as the microphone and environment sensors (e.g. humidity, temperature, and pressure sensors) to interact with the environment. In such applications, the unsealed chamber is required for MEMS devices encapsulated by the wafer level capping technique.

Various approaches have been reported to realize multiple chamber pressures for combo sensors (SoC), such as by adopting thin film getters [11], by varying chamber volumes at different substrate approaches [12, 13], and by using the sensor design and bonding sequences [14, 15]. Moreover, the concept to realize sealed chamber with low pressure and unsealed chamber with ambient pressure for combo sensors (SoC) has been demonstrated by wafer level thin film encapsulation [16] and air path formation at the capping side of wafer level packaging [17], but large opening for the air path could cause the stiction of suspended MEMS structures by the wet processes after wafer level packaging (water or particles penetrate into the unsealed chamber). Nevertheless, the requirements of extra materials and additional fabrication processes are important concerns for the application of the

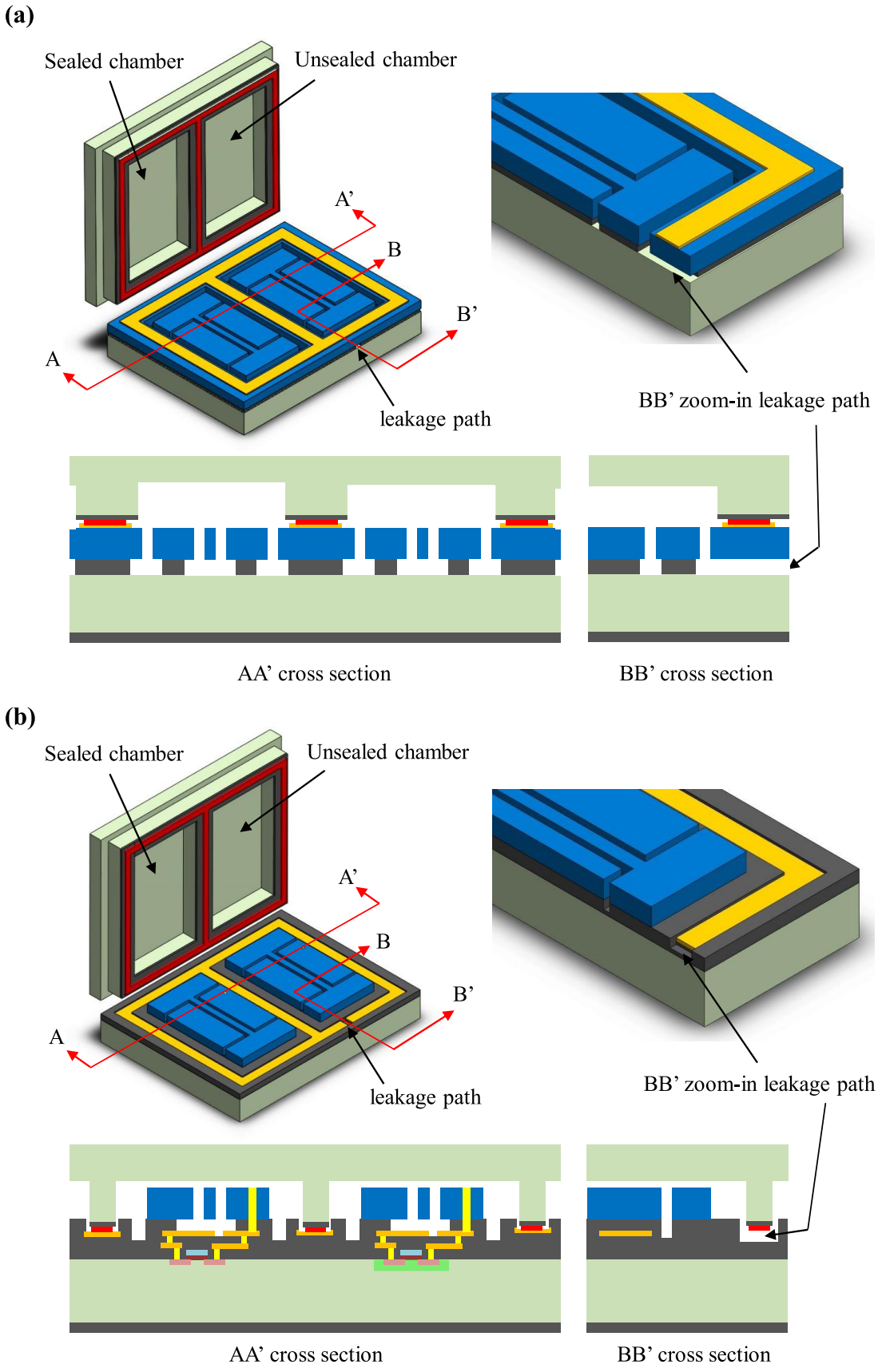


Figure 2. Extending the existing BOD and BOC platforms without additional process steps to realize sealed and unsealed chambers by using the proposed leakage path designs, (a) the leakage path on oxide layer is proposed for the BOD platform, and (b) the leakage path on the metal/oxide layers is proposed for the BOC platform.

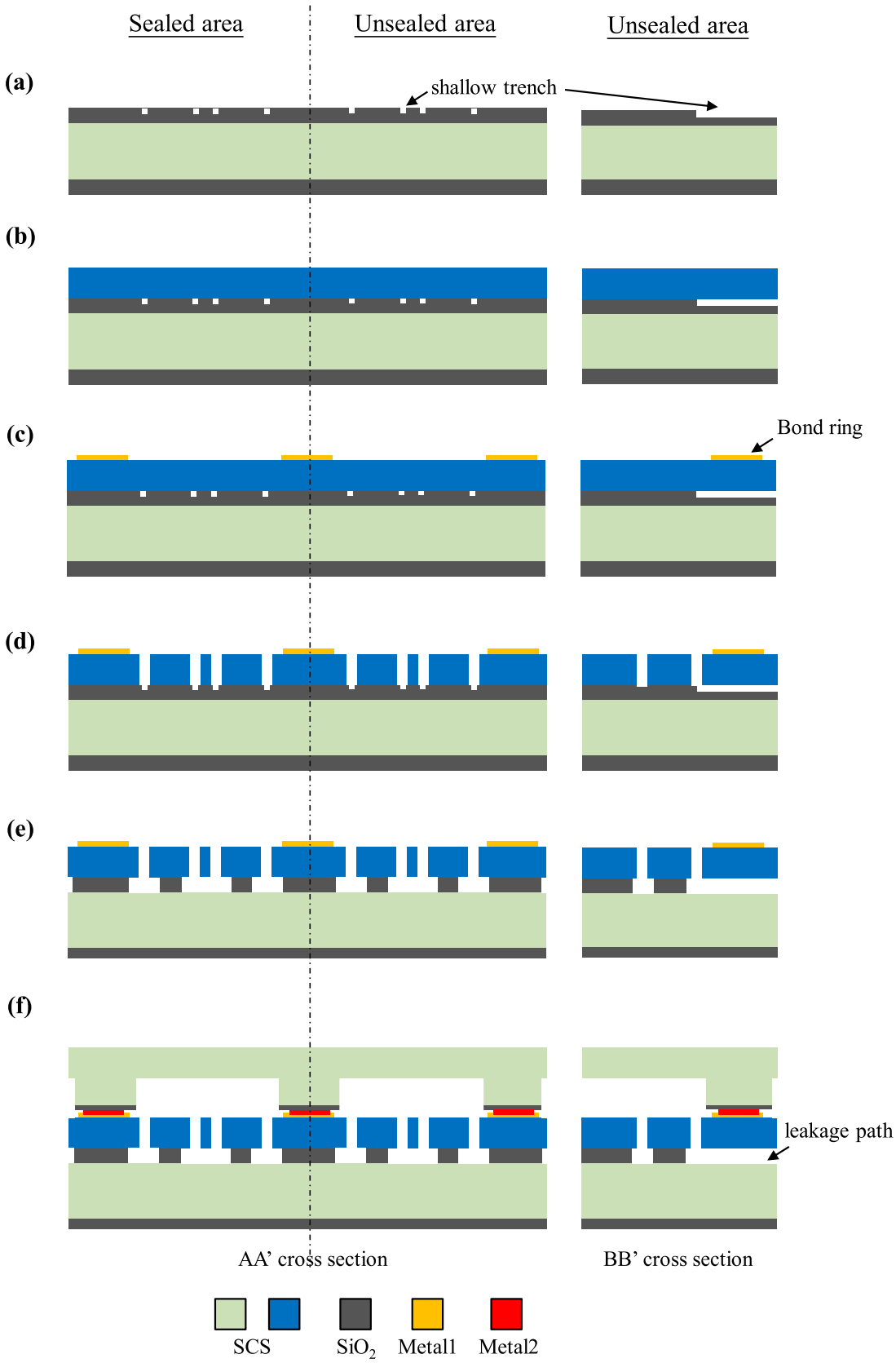


Figure 3. The BOD fabrication process steps to implement the present concept: (a) wafer started with thermal oxidation as the sacrificial layer and shallow trenches were patterned to define the MEMS release area and the leakage paths; (b) another silicon substrate (MEMS device layer) was bonded to oxide (fusion bonding) and then annealed; (c) after the wafer thinning processes to define the thickness of MEMS device layer, the metal film was sputtered and patterned to define the electrical connect and bonding rings; (d) the MEMS structures were patterned by the DRIE process; (e) the VHF was used to release MEMS structures and also fully open the leakage paths; (f) the substrate with MEMS devices was encapsulated by wafer level eutectic metal bonding.

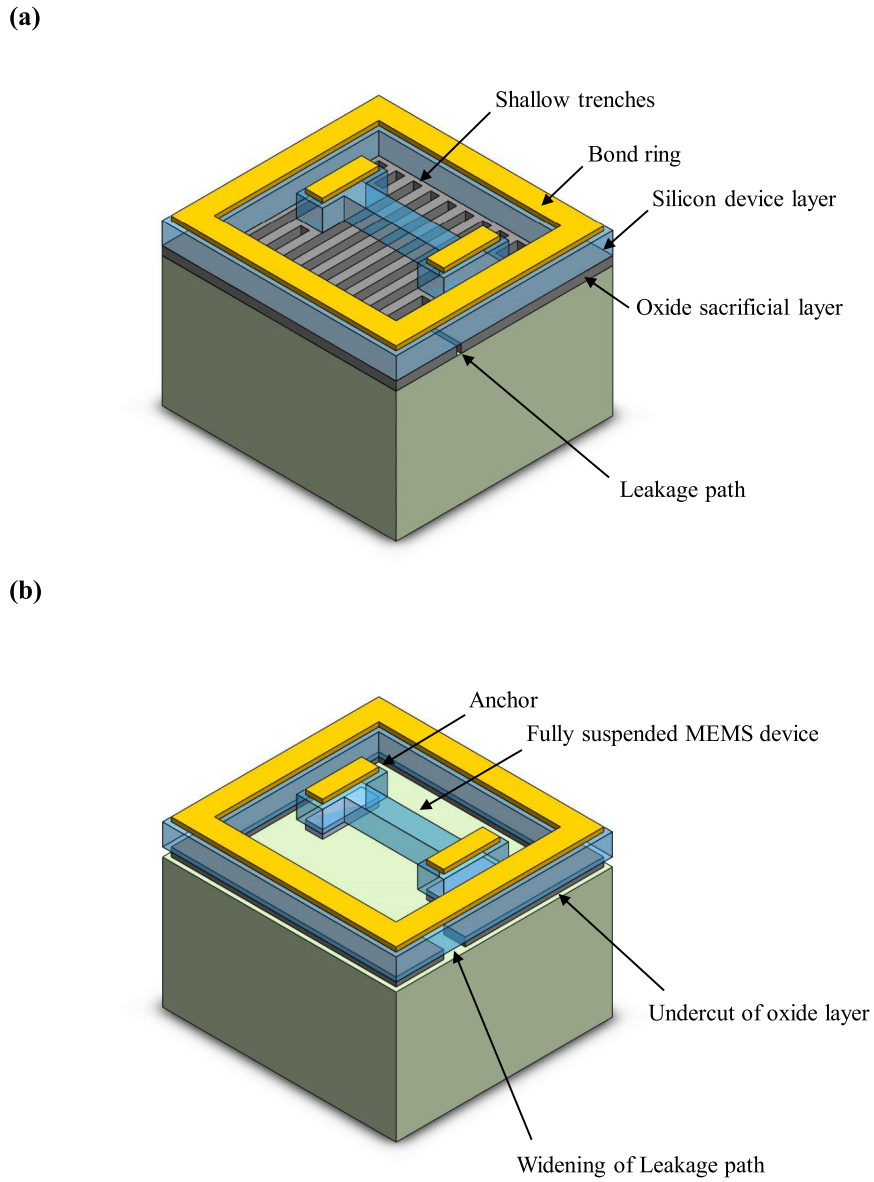


Figure 4. The shallow trenches (defined in figure 3(a)) (a) before, and (b) after the VHF MEMS release process, addressing their importance to reduce the releasing time of MEMS structures and leakage paths for the BOD platform.

above approaches. Based on the TSMC two existing commercial MEMS process platforms shown in figure 1 [3, 18], this study presents SoC approaches to realize combo sensors and respectively encapsulated in sealed and unsealed chambers without additional processes and materials. As shown in figure 1(a), the process platform with capping wafer bonded on the MEMS device layer named BOD (bond on device layer). As shown in figure 1(b), the process platform with capping wafer bonded on the carrier substrate named BOC (bond on carrier substrate). Note that the carrier substrate in figure 1(b) is a CMOS chip. The detail process information for BOD and BOC is summarized in table 1. These two foundry available process platforms are established for different applications. The major contribution of this study is to present simple approaches to realize both sealed and unsealed chambers after wafer level packaging. The concept could extend to other process platforms for various applications.

2. The design concepts and process flows

As shown in figure 1, the existing BOD and BOC process platforms could fabricate MEMS devices and further seal them in chambers. This study presents the concept to leverage the same process steps to fabricate MEMS devices and then respectively encapsulates them in sealed and unsealed chambers. Thus, the approach could enable the integration of MEMS sensing devices in the sealed chamber (e.g. motion sensors) and unsealed chamber (e.g. environment sensors) for comb sensors SoC. Figure 2 shows the proposed architectures of capping devices for both BOD and BOC process platforms. The concept of forming the sealed chamber and unsealed chamber simultaneously is to design the leakage paths depicted in figures 2(a) and (b). Thus, the unsealed chamber could connect to the ambient through the leakage path after hermetic wafer bonding. As shown in figure 2(a),

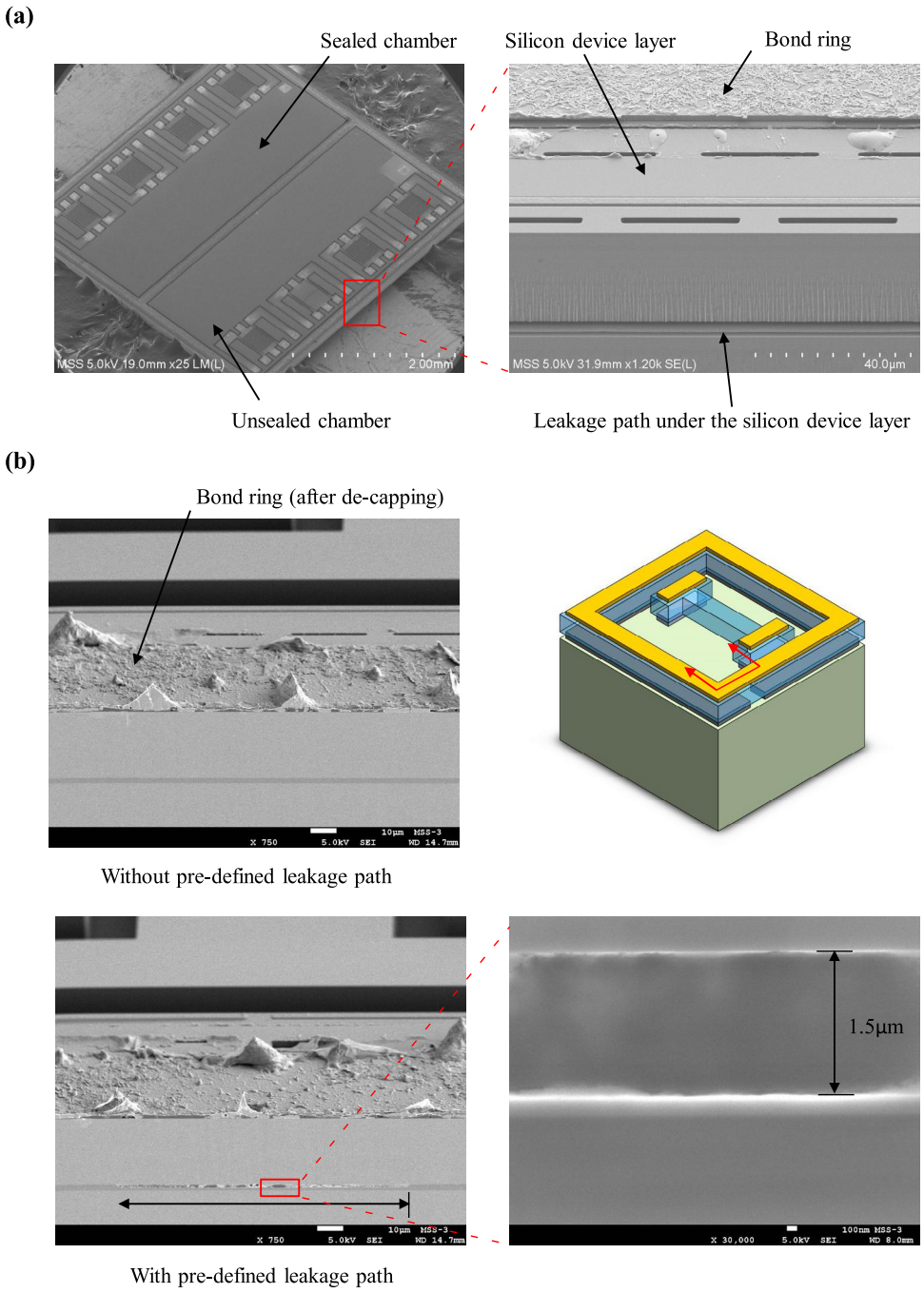


Figure 5. Typical fabrication results after the BOD process, (a) SEM micrograph indicates the sealed and unsealed chambers on the same chip after de-capping. The sacrificial oxide undercut is observed, but the leakage path beneath the bond ring is invisible, and (b) polishing the chip to the middle bond ring plane, the pre-defined leakage path is observed, and the comparison with the no pre-defined leakage path sample is also available. The zoom-in micrograph shows the leakage path with 1.5 μm height.

the leakage path for BOD process platform is a shallow trench (or shallow trenches, with the trench dimensions of 20–100 μm wide, 1.5 μm deep, and 80 μm long) defined at the oxide layer. Moreover, as shown in figure 2(b), the leakage path for BOC process platform is also a shallow trench (or shallow trenches, with the trench dimensions of 20–100 μm wide, 1.5 μm deep, and 80 μm long) defined at the metal layer. The shallow trenches enable the connection of encapsulated chamber and the ambient after the wafer level capping process. Note that no additional processes are required to pattern the oxide and metal shallow trenches. The detailed process steps to implement the capping devices in figure 2 are presented as follows.

2.1. BOD process flow

The process integration sequences to simultaneously fabricate the sealed and unsealed chambers for BOD are illustrated in figure 3 (the AA′ & BB′ cross-sections depicted in figure 2(a)). As shown in figure 3(a), the thermal oxide was grown on the initial carrier substrate to act as the fusion bonding interface and also the sacrificial layer for the following etching release

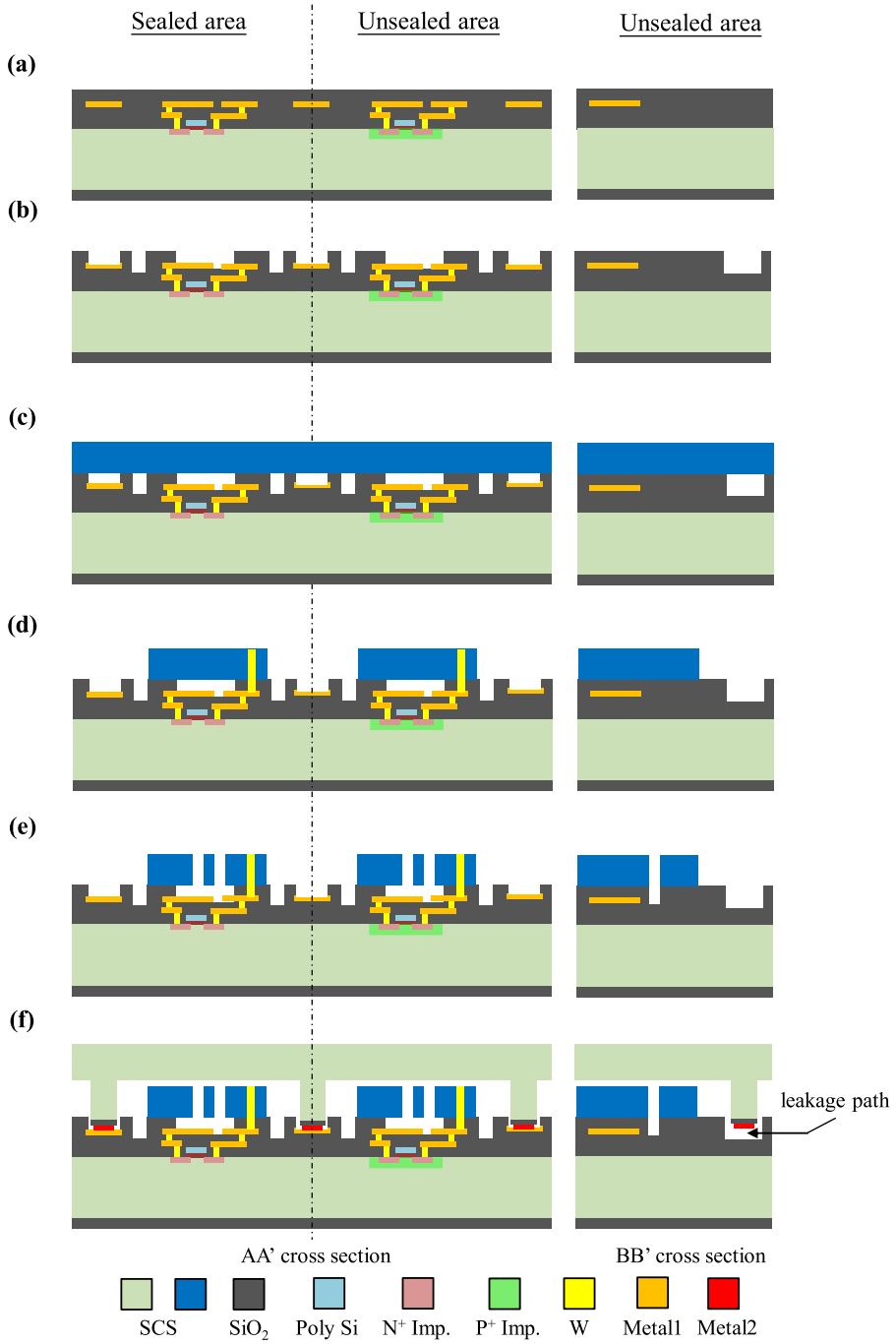


Figure 6. The BOC fabrication process steps to implement the present concept: (a) the carrier substrate is defined by either CMOS circuitry or metal routings for electrical connect only. The top metal layer is patterned for routings, IO pads, and bonding ring. The non-closed bond ring is defined in advance also. Top oxide deposition and planarization for rest silicon-to-oxide fusion bonding purpose; (b) the cavity, IO pads, and bond ring area exposed by lithography and etching steps; (c) another silicon substrate (MEMS device layer) prepared for wafer fusion bonding and annealing; (d) wafer thinning processes to form the MEMS device layer target thickness (i.e. 5–30 μm). After that, deep via patterned, stopping on the top metal layer and W filling for electrical connect; (e) planar MEMS structures defined and bonding rings exposed by DRIE; (f) prepared cavities of capping wafer and wafer level eutectic metal bonding.

process. After that, the shallow trenches were patterned by the dry etching. Note that the original purposes of shallow trenches are: (1) to offer sufficient bonding area/strength for the following processes such as silicon grinding, and (2) to shorten the etching release time for MEMS structures. This study further employs this process step to define the leakage paths for the unsealed chamber. As illustrated in figure 3(b), the thin single crystal silicon device layer (serving as the MEMS structure layer) was formed by using the wafer fusion bonding and annealing to increase the bonding strength. As depicted in figure 3(c), the thickness of the MEMS structure layer is tunable by the thinning process sequences like wet etching, wafer grinding, surface polishing, and so on, depending on sensors design requirements. After that, surface cleaning and metal sputtering were processed to ensure the metal to silicon interface ohmic contact, and then the metal

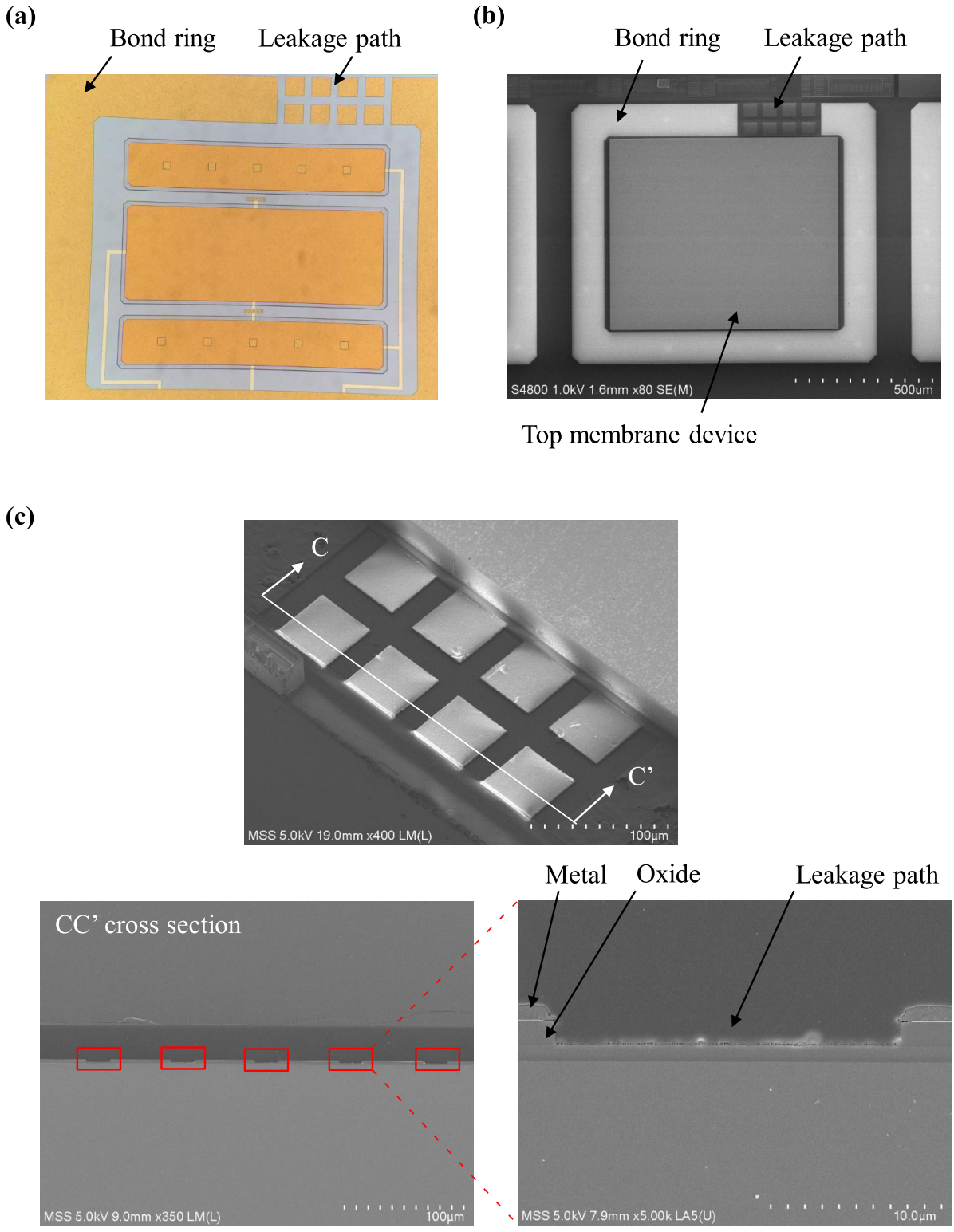


Figure 7. SEM micrographs of the inline process observation (a) the result after the process in figure 6(b) to show the exposed metal layer for bonding ring and the area without metal film is defined as the leakage path for the unsealed chamber, (b) the result after the process in figure 6(e) to show the bonding ring and the MEMS device before wafer eutectic bonding process, and (c) the zoom-in and cross-section views of the leakage path.

bond ring was defined for the following metallic (Al–Ge) eutectic bonding. As shown in figure 3(d), the single crystal silicon device layer was patterned to define the in-plane dimensions of main MEMS structures by the DRIE (deep reactive ion etching) process. As illustrated in figure 3(e), the MEMS structures were suspended after removing sacrificial oxide by vapor phase hydrofluoric acid etching (VHF). The shallow trenches (served as the etching release trenches) and leakage path pre-defined by the process in figure 3(a) play important roles in this process, as depicted in figure 4. The

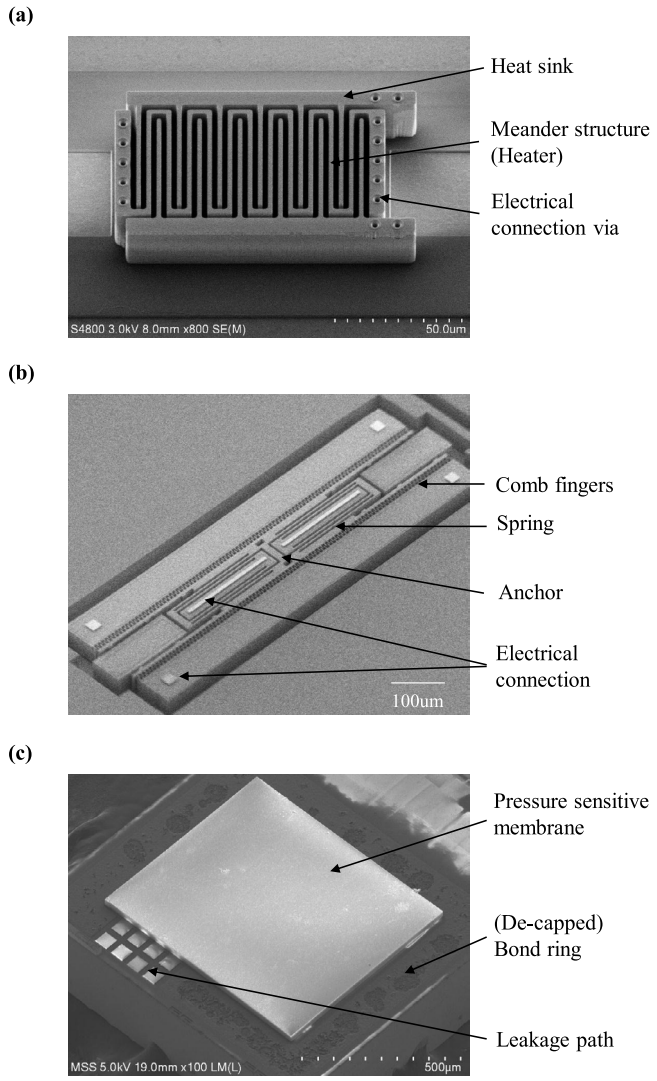


Figure 8. The three pressure sensitive sensors fabricated and embedded in the chambers to evaluate the approaches presented in this study, (a) micromachined Pirani gauge, (b) mechanical resonator, and (c) capacitive pressure sensor.

VHF could penetrate the shallow trenches under the silicon device layer to undercut the sacrificial SiO_2. Thus, the etching time to fully open the leakage path and to fully suspend the MEMS structures is significantly reduced. Note that the leakage path was expanded due to the VHF etching. Finally, the eutectic metal bonding was adopted to form the wafer level packaging shown in figure 3(f). As a result, the sealed and unsealed chambers were simultaneously achieved after the eutectic bonding process to offer two different chamber pressures, and no extra process steps are required. The scanning electron microscopy (SEM) micrograph in figure 5(a) displays the typically fabricated chip by BOD process with sealed and unsealed chambers. The zoom-in micrograph indicates the location of the leakage path under the silicon device layer and the bonding ring. Note the leakage path is hidden by the silicon device layer, yet the undercut of the oxide layer by VHF process (as indicated in figure 4(b)) can be observed. Micrographs in figure 5(b) further show the chips which were polished to look into the leakage path (around 100 μm wide and 1.5 μm deep) underneath the bonding ring. The micrographs in left-hand side respectively depict the chips without and with pre-defined leakage path. The sample with leakage path will trap the residual resulted from the polishing process, however, the sample without leakage path is clean.

2.2. BOC process flow

As shown in figure 6 (the AA′ and BB′ cross-sections depicted in figure 2(b)), this study extends the silicon above CMOS process scheme [3] to simultaneously fabricate the sealed and unsealed chambers for BOC. As shown in figure 6(a), the initial carrier substrate was prepared by using the standard CMOS processes. The surface of the CMOS wafer was covered with the metal and dielectric layers. The top oxide passivation was used to define the moving space for the suspended MEMS devices in the following process. Moreover, the top metal film was acted as the layer for the following eutectic bonding process. Thus, this study presents the concept to define the sealed and unsealed regions by patterning the top metal layer. No extra process steps are required. As illustrated in figure 6(b), the top dielectric layer was patterned to define the spacers, meanwhile, the top metal layer was exposed. Note that no metal layer (etching stop layer for the dielectric film) was defined in the BB′ cross-section region. Therefore, the etching depth of the dielectric layer in the BB′ cross-section region was used to determine the depth of the leakage path. As shown in figure 6(c), the second silicon substrate for the MEMS structure layer was bonded on the CMOS wafer. After that, as displayed in figure 6(d), the wafer thinning process was used to define the thickness of MEMS structures and then the electrical connections between CMOS chip and MEMS structures were fabricated by using the deep via etching and metal filling processes. As depicted in figure 6(e), the deep silicon etching was used to define the MEMS structures and also to expose the bonding area and the leakage paths. Finally, as illustrated in figure 6(f), the Al–Ge eutectic bonding was employed to form the wafer level packaging. The bonding regions and leakage paths were respectively defined by the areas with and without the top metal layer (as depicted in figure 6(b)). As a result, the sealed and unsealed chambers were simultaneously achieved after the eutectic bonding process to offer two different chamber pressures, and no extra process steps are required. Figure 7 shows typical fabrication results. The micrograph in figure 7(a) displays the process result in figure 6(b). The bonding ring and leakage paths defined by the top metal layer are observed. Moreover, the top metal layer patterned as the sensing electrodes for capacitive type pressure sensor is also observed. The SEM micrograph in figure 7(b) shows the process result in figure 6(e). The MEMS structure (membrane) is bonded on the CMOS chip with sensing electrodes to implement the pressure sensor. Since the sensor will expose the ambient for pressure detection, the leakage path depicted in the micrograph is required to achieve the unsealed chamber after the following wafer level packaging. Figure 7(c) further depicts the close views of the leakage paths before wafer bonding. The left cross-section micrograph

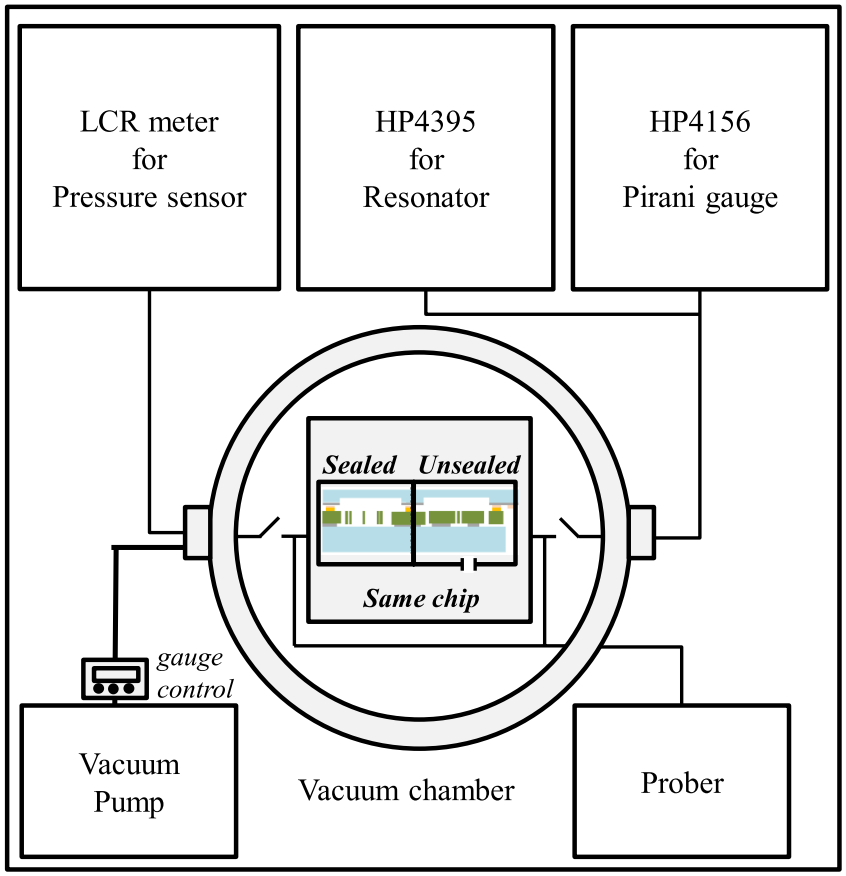


Figure 9. Schematic of the test setup including the PCC to accommodate the 8-inch wafer, manual probers, and three peripheral measurement tools for the signal extraction of different pressure sensitive devices such as, HP4156 for the resistance change (micromachined Pirani gauge), HP4395 for the impedance change (mechanical resonator), and LCR meter for the capacitance change (pressure sensor).

shows the presented design has leakage paths with five small trenches. The right zoom-in cross-section micrograph further depicts the 20 μm wide 1.5 μm deep trench with metal and oxide layers on its sidewalls. The net width of these 5 leakage paths is 100 μm. Note that the number and width of trenches can be increased to enlarge the net width of leakage paths.

In summary, the present approaches exploit the same process flow and sequence of mask layers to simultaneously implement sealed and unsealed chambers for BOD and BOC platforms. To demonstrate the feasibility of the present approaches, the pressure sensitive sensors have been implemented and encapsulated through the BOD in figure 3 and the BOC platforms in figure 6. Figure 8 shows three typical devices including Pirani gauge, resonator, and capacitive pressure sensor, implemented in this study for pressure monitoring. The micromachined Pirani gauge is a simple sensing unit for *in situ* vacuum condition [19, 20] and even atmospheric pressure [21] monitoring. According to the analytical model in [22], the Pirani gauges have been designed and fabricated. The SEM micrograph in figure 8(a) shows a typical fabricated Pirani gauge. The meander structure (2 μm wide) is designed as the heater and the interdigitated fingers distributed in between the heater are acted as the heat sink. The gap between the heater and the heat sink is ~2 μm. As shown in figure 8(b), the micromachined resonator with quality factor sensitive to the ambient pressure is also implemented using BOD platform for the demonstration of device integration and chamber sealing condition evaluation [23]. In addition, the capacitive type absolute pressure sensor is designed into the BOC scheme, as shown in figure 8(c).

3. Experiment results and discussions

For the validation of the presented approaches, the study employs the measurement setup in figure 9 to characterize the fabricated devices to evaluate the pressure of sealed and unsealed chambers. As indicated in the figure, the 8-inch wafer with fabricated chips is placed inside a pressure control chamber (PCC) for wafer level testing and mapping. The vacuum condition of PCC is controlled by the dry scroll pump and turbopump to achieve a pressure level of 1.0×10^{-4} Torr. The input driving and output sensing signals are transmitted through probers. For the Pirani gauge tests, the peripheral measurement tool HP4156 is operated at constant driving voltage mode to extract the resistance change of sensor with respect to the pressure variation of the environmental chamber. Firstly, this study characterized the resistance change of Pirani gauges encapsulated by the sealed and unsealed chambers at different PCC pressure. The typical measurement results in figure 10 depict the normalized

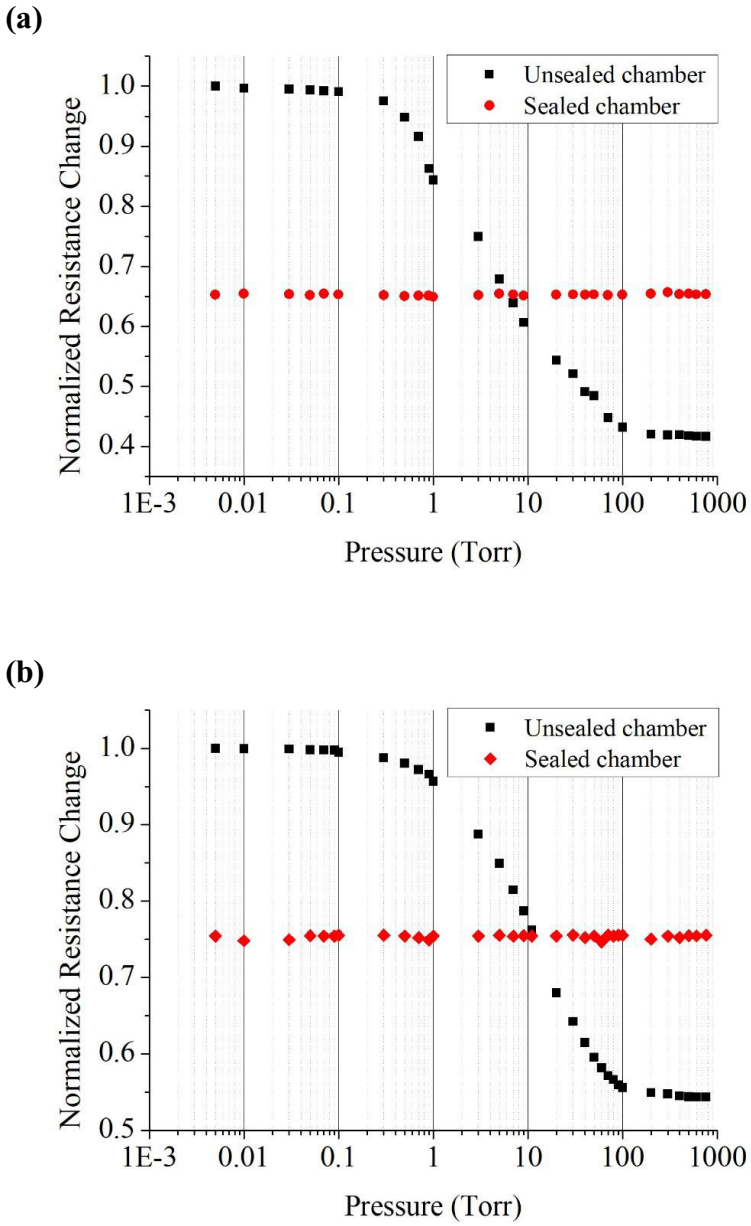
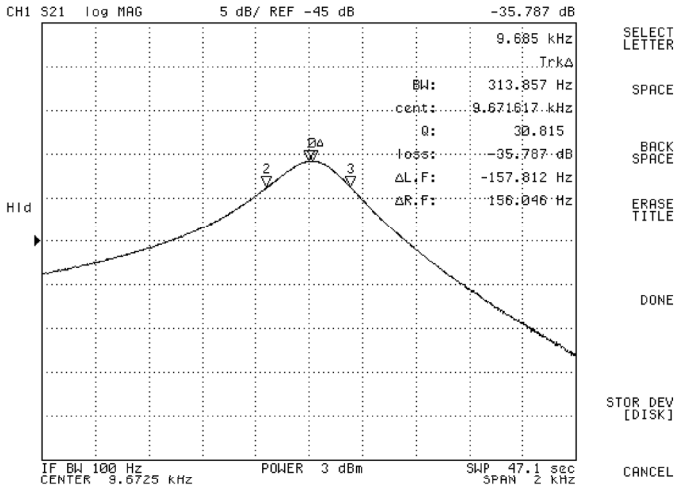


Figure 10. Typical measurement results of the micromachined Pirani gauge to show the normalized resistance change versus different pressure conditions of PCC for the unsealed and sealed chambers fabricated by (a) BOD platform, and (b) BOC platform.

resistance change of Pirani gauge versus the vacuum condition of PCC. Figure 10(a) shows the results for Pirani gauges implemented and encapsulated through the BOD scheme. According to the measurements, as the vacuum condition of PCC changed, the pressure of the unsealed chamber changed with it whereas the pressure of the sealed chamber remained at around 5 Torr (the initial pressure). The results agree well with the prediction and demonstrate the present process could enable the realization of sealed and unsealed chambers for the BOD scheme. Moreover, figure 10(b) depicts the results for Pirani gauges implemented and encapsulated through the BOC scheme. Similarly, the pressure of the unsealed chamber changed with that of PCC whereas the pressure of the sealed chamber remained at around 10 Torr (the initial pressure). The results also show the present approach could enable the realization of sealed and unsealed chambers for the BOC scheme.

Secondly, this study designed and implemented typically moving MEMS structures (i.e. capacitive type MEMS resonators) by using the BOD scheme, and further exploited the encapsulated micro-resonators as the test key to evaluate the vacuum condition of sealed and unsealed chambers. The damping of the micro-resonator is highly sensitive to the ambient pressure, and hence the quality factor of the resonation is a good indicator to monitor the chamber pressure. As depicted in figure 9, the network analyzer HP4395A is used to determine the dynamic responses of the resonator, and further find out its natural frequencies and quality factor. Figure 11(a) shows a typically measured frequency response of the resonator encapsulated inside a sealed chamber. In this case, the resonator is sealed in a chamber of 10 Torr, and the quality factor determined from the measurement is 30. Measurements in figure 11(b) further show the variation of the the quality

(a)



(b)

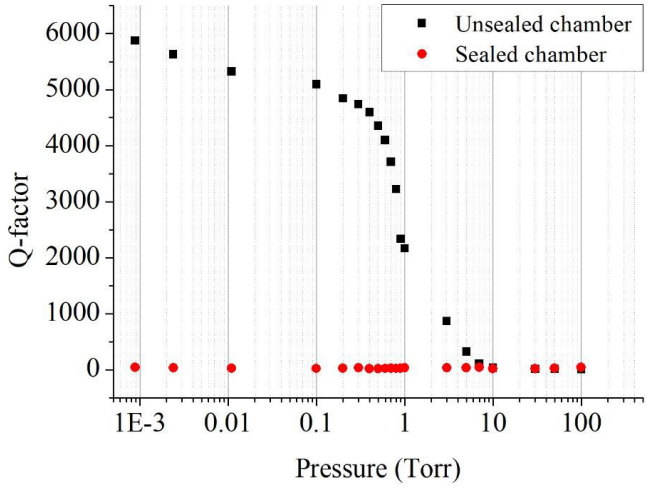


Figure 11. Typical measurement results of the mechanical resonator fabricated by the BOD platform, (a) the frequency response of resonator encapsulated inside a sealed chamber with a pressure of 10 Torr, and the quality factor determined from the measurement is 30, (b) quality factors respectively extracted from devices in unsealed and sealed chambers with different PCC pressure conditions.

factor for the sealed and unsealed chambers when the PCC pressure varying from 100 Torr to 1.0×10^{-3} Torr. The results indicate that the quality factor of the resonator encapsulated inside the unsealed chamber increases from 30 to 5000 as the PCC pressure dropped from 10 to 0.2 Torr. However, the quality factors have no significant change when for the resonators encapsulated inside the sealed chambers. The measurements show that the present approach could simultaneously fabricate and encapsulate MEMS devices inside sealed and unsealed chambers through wafer level BOD scheme.

Finally, this study also fabricates the capacitive type pressure sensor on the BOC scheme and encapsulates it inside the unsealed chamber. The functional tests of the pressure sensor inside the unsealed chamber are characterized by using the LCR meter. Measurements in figure 12 show the variation of sensing capacitance with the PCC pressure (within the range of 225–900 Torr, equivalent to 300 hPa–1200 hPa, for practical barometric measurement applications). The BOC scheme has been successfully demonstrated the implementation and encapsulation (in the sealed chamber) of motion sensors [24].

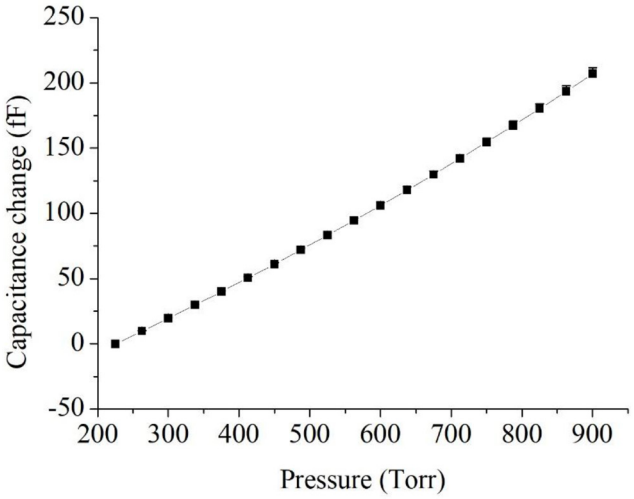


Figure 12. The functional tests of the capacitive pressure sensor encapsulated inside the unsealed chamber fabricated by the BOC platform. The sensing signals varying with vacuum conditions of PCC demonstrates that the present approach enables the BOC platform to integrate motion and environmental hubs.

According to the presented approach, the BOC scheme could integrate the motion sensors (in the sealed chamber) and the pressure sensor (in the unsealed chamber) through the wafer level packaging for broad applications. Moreover, the three different pressure sensitive sensors were characterized after completing wafer level fabrication including the final wafer grinding and dicing processes (which employing the water jetting for removing particles and also for cooling). The normal function of these three sensors indicates that the leakage path design could tolerate the processes with water jetting and also prevent the damage of sensors inside the chamber.

4. Conclusions

This study has demonstrated the approaches to extend two existing commercial MEMS fabrication platforms by embedding leakage paths at the wafer bonding interface. Thus the sealed and unsealed chambers with different chamber pressure conditions are simultaneously achieved after the wafer level packaging. The lower pressure in the sealed chamber is controlled by the vacuum condition during the bonding process and the pressure inside the unsealed chamber changes with the ambient pressure. Moreover, the sensing or actuating devices inside the unsealed chamber could expose to the ambient. By integrating with the technology in [13], the motion sensors and environmental sensors can be integrated on the same chip. In summary, the presented process schemes (BOD and BOC) offer simple approaches to realize both sealed and unsealed chambers after wafer level packaging. No extra fabrication and materials are required which are especially important for commercial applications. The concept could extend to other process platforms for various applications. Note that the parameters such as the number and dimensions of the trenches will change the performances of the unsealed chamber, for instance, the bonding strength and the response time of the chamber pressure with the ambient pressure variation [25]. These design parameters need to be optimized based on the specifications of future applications.

In this study, the thermal oxide layer is employed to realize the shallow trenches for the BOD process. In comparison, the shallow trenches could be defined at the metal layers in figure 3. However, in this approach, it is difficult to control the depth of the shallow trench due to the deformation of metal layers by the high temperature and bond force eutectic bonding process. This study has designed and implemented three pressure sensitive devices, the Pirani vacuum gauge, the mechanical resonator, and the capacitive pressure sensor, by using the BOC and BOD schemes to demonstrate the presented concept. The Pirani gauges have been fabricated by both BOC and BOD schemes. Measurements indicated that the resistance of Pirani gauge inside the unsealed chamber varies with the ambient pressure. Moreover, the flexure mode mechanical resonators have been designed and realized using the BOD scheme. Measurements show that, as ambient pressure dropped from 10 Torr to 0.2 Torr, the quality factor of resonator inside the unsealed chamber increases from 30 to 5000, whereas the quality factor of the resonator inside the sealed chamber remains 30. Finally, the capacitive pressure sensors are fabricated by the BOC scheme. As depicted in the experiment results, the capacitance change with the ambient pressure from 225 to 900 Torr of the barometric application range for the capacitive pressure sensor in the unsealed chamber, extending the applications of BOC platform for the SoC integration of multiple sensors. Thus, the same concept could also apply to the BOD platform. The Pirani gauge and mechanical resonator sensor have different pressure sensitive ranges, and hence can be fabricated inside the sealed chambers to serve as the *in situ* pressure monitoring components.

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