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Realize multiple hermetic chamber pressures for system-on-chip process by using the capping wafer with diverse cavity depths

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Abstract

Many mechanical and thermal characteristics, for example the air damping, of suspended micromachined structures are sensitive to the ambient pressure. Thus, micromachined devices such as the gyroscope and accelerometer have different ambient pressure requirements. Commercially available process platforms could be used to fabricate and integrate devices of various functions to reduce the chip size. However, it remains a challenge to offer different ambient pressures for micromachined devices after sealing them by wafer level capping (WLC). This study exploits the outgassing characteristics of the CMOS chip to fabricate chambers of various pressures after the WLC of the Si-above-CMOS (TSMC 0.18 μm 1P5M CMOS process) MEMS process platform. The pressure of the sealed chamber can be modulated by the chamber volume after the outgassing. In other words, the pressure of hermetic sealed chambers can be easily and properly defined by the etching depth of the cavity on an Si capping wafer. In applications, devices sealed with different cavity depths are implemented using the Si-above-CMOS (TSMC 0.18 μm 1P5M CMOS process) MEMS process platform to demonstrate the present approach. Measurements show the feasibility of this simple chamber pressure modulation approach on eight-inch wafers.

Keywords: wafer level capping, hermetic, outgassing, MEMS

(Some figures may appear in colour only in the online journal)

1. Introduction

Micro-electromechanical systems (MEMS) technology has been extensively employed to implement semiconductor-based sensors for the applications of consumer electronics, automotive systems, environmental monitoring, medical diagnostics, etc. To reduce the process cost, foundries have used the concept of the process platform in the semiconductor industry in the fabrication of MEMS devices. Presently, various process platforms are available, such as THELMA (thick epitaxial layer for micro gyroscope and accelerometer) of STMicroelectronics [1], the micro electro mechanical systems silicon on insulator (MEMSOI) platform of Tronics [2], and the Si-above-CMOS (complementary metal oxide semiconductor) platform of the Taiwan Semiconductor Manufacturing Company (TSMC) [3]. Thus, various MEMS devices can be batch-fabricated and also integrated in a monolithic manner using the process platforms. For instance, the integration of accelerometers and gyroscopes has been demonstrated in various applications [4, 5]. In addition to the fabrication of MEMS devices, the wafer-level integration of CMOS circuits can also be achieved using the bonding

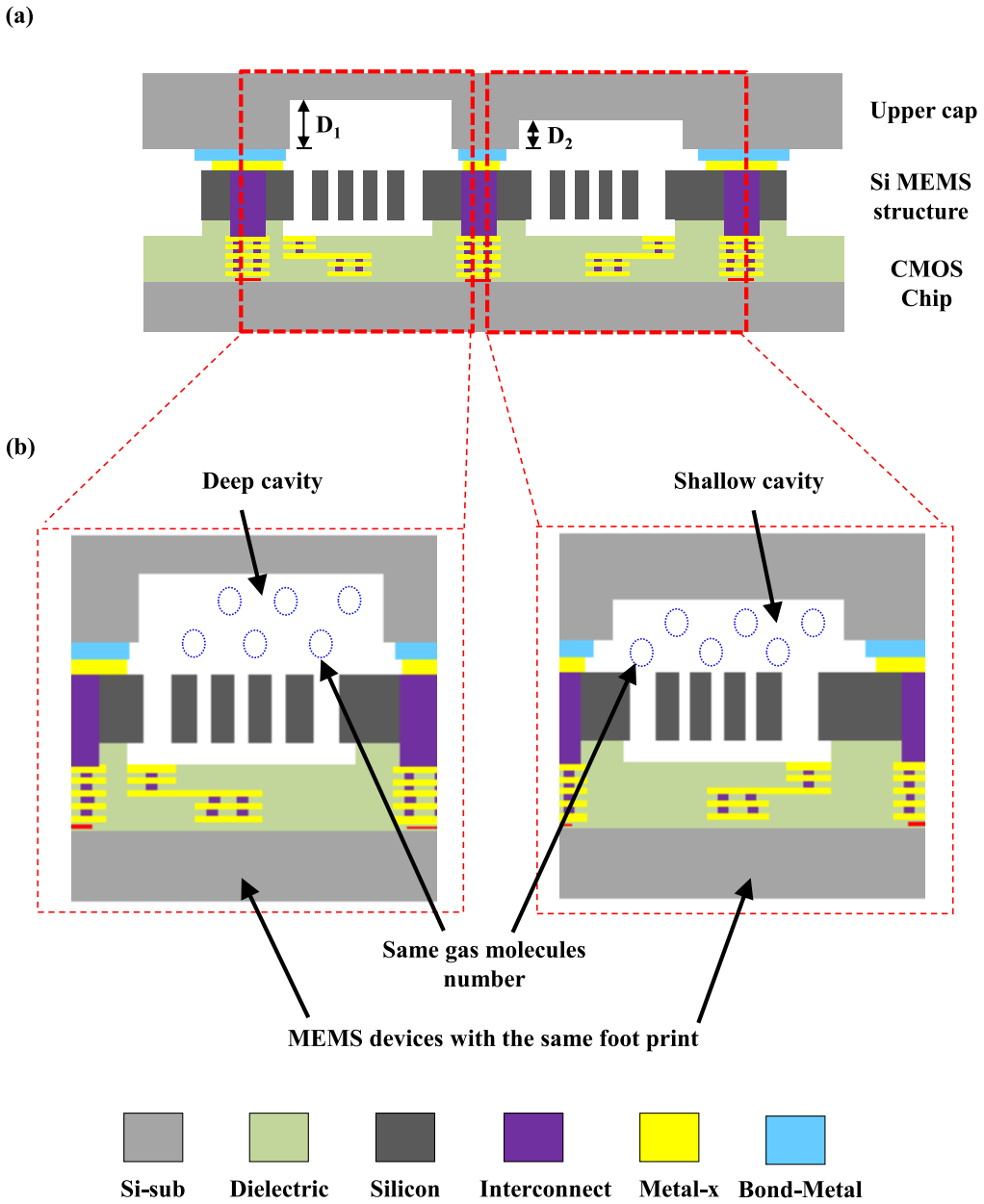


Figure 1. Design concept of the presented study: (a) the MEMS devices are hermetically sealed by the Si caps with different cavity depths, using the WLC process; (b) the outgassing of the wafer will increase the chamber pressure, and such pressure variation could be modulated by varying the chamber volume (i.e. cavity depth).

process, as demonstrated by TSMC's Si-above-CMOS platform [3]. Moreover, after the micro fabrication processes, the suspended MEMS devices can be further protected by a silicon cap, using the wafer-level-capping (WLC) bonding process. Thus, damage is prevented during the dicing process that follows. The aforementioned process platforms are the key enabling step to achieve the system on chip (SoC). Compared with system-in-package (SiP) technology, the SoC solution could offer advantages in several aspects such as the device footprint, parasitic connection, power consumption, and manufacturing cost.

In general, MEMS devices contain moving structures to interact with excitations from the environment and further produce corresponding output signals. These suspended micro structures are extremely sensitive to the ambient pressure and hermeticity during operation [6]. Moreover, during the operation of MEMS devices, the moving structures have different ambient pressure requirements to improve their performances. For example, atmospheric or low-vacuum conditions are required for accelerometers to provide air damping [7], yet a high vacuum is required for a gyroscope or resonator to enhance its quality factor [8]. In general, the ambient pressures for the operation of accelerometer and gyroscope have nearly a 10-fold difference [9]. As a result, the resonators, gyroscopes, digital micro mirrors, and microfluidic devices are packaged in specific ambient pressure conditions to meet operational requirements. In addition, to ensure the performance of MEMS devices, stable ambient conditions are required, such as pressure. The controllable chamber pressure and hermeticity provide a required Q value of mechanical vibration, with sufficient stability to protect MEMS devices from mechanical damage and contamination.

Table 1. Summary of the measurements showing that hydrogen is the major outgassing on CMOS and Si capping wafers. The outgassing of the CMOS wafer is one order of magnitude higher than that of Si capping wafers with different cavities.

Residue gas analyzer		Pressure (Torr)		
Gas	Temperature (°C)	CMOS	Si cap with 137.7 μm cavity	Si cap with 10.3 μm cavity
Hydrogen	350	3.80×10^{-4}	2.30×10^{-6}	2.30×10^{-6}
	400	5.20×10^{-3}	2.50×10^{-6}	2.4×10^{-6}
Structure		AlCu CVD OX	137.7μm	10.3μm

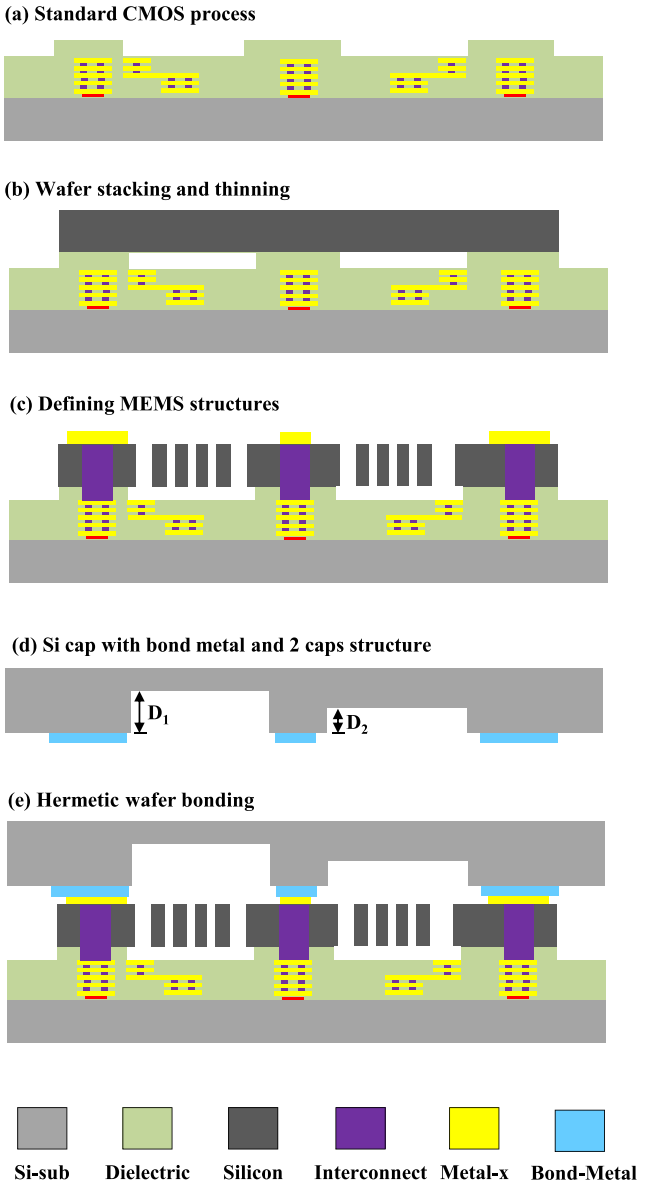


Figure 2. The fabrication process steps. (a) Define cavity and bump areas of CMOS chip. (b) Bond Si wafer on CMOS chip and then thin the Si wafer to the required thickness for the MEMS device. (c) Define the MEMS devices and their vias and the bond metal for Si capping. (d) Define the cavities with different depths on the Si cap. (e) Seal the MEMS devices by the WLC process, using eutectic bonding.

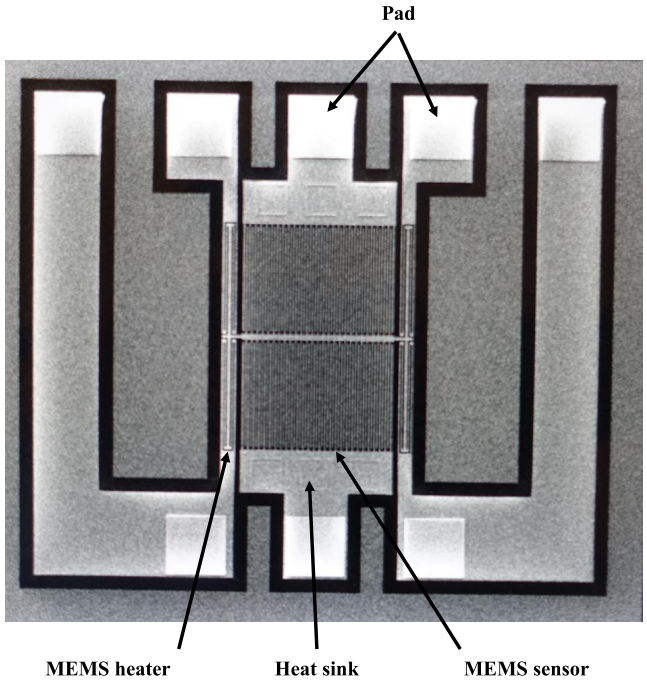


Figure 3. Scanning electron microscopy of a typical fabricated Priani gauge embedded inside the hermetic chamber for pressure monitoring.

The wafer-level package technologies for the encapsulation of MEMS devices have been extensively investigated and reported [10–15]. The pressure of the hermetically sealed chamber for MEMS devices is specified during the WLC process. For the SiP solution [16–18], the MEMS devices, such as accelerometer and gyroscope, are fabricated in different wafers. Thus, the different ambient pressure requirements of these MEMS devices can be easily specified by the WLC process on separate wafers. On the other hand, various MEMS devices are fabricated and integrated on the same wafer using the SoC approaches, for instance the integration of accelerometer and gyroscope [4, 5]. It is challenging to specify various ambient pressures for these monolithically integrated MEMS devices (such as accelerometer and gyroscope) by using the WLC process. The getter material has been employed to change the pressure of the sealed chamber [19]. However, limited pressure variation, high material process cost, difficult getter pattern definition, and high sensitivity to the WLC bond process are all concerns for the getter material. The approach

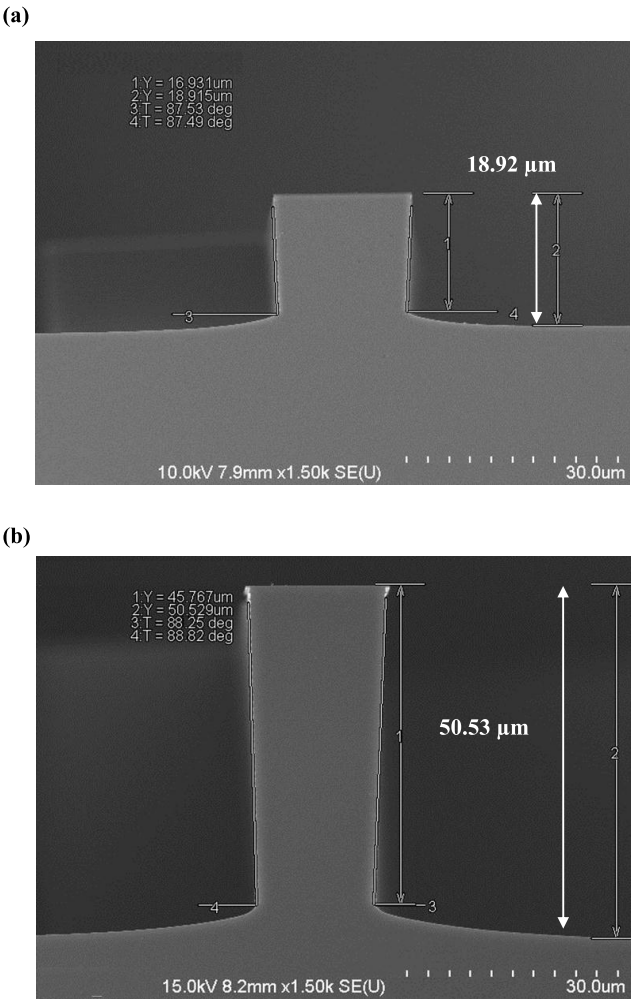


Figure 4. SEM micrographs showing the cross-sections and measured depths of two cavities: (a) the cavity of 18.9 μm depth, and; (b) the cavity of 50.5 μm depth.

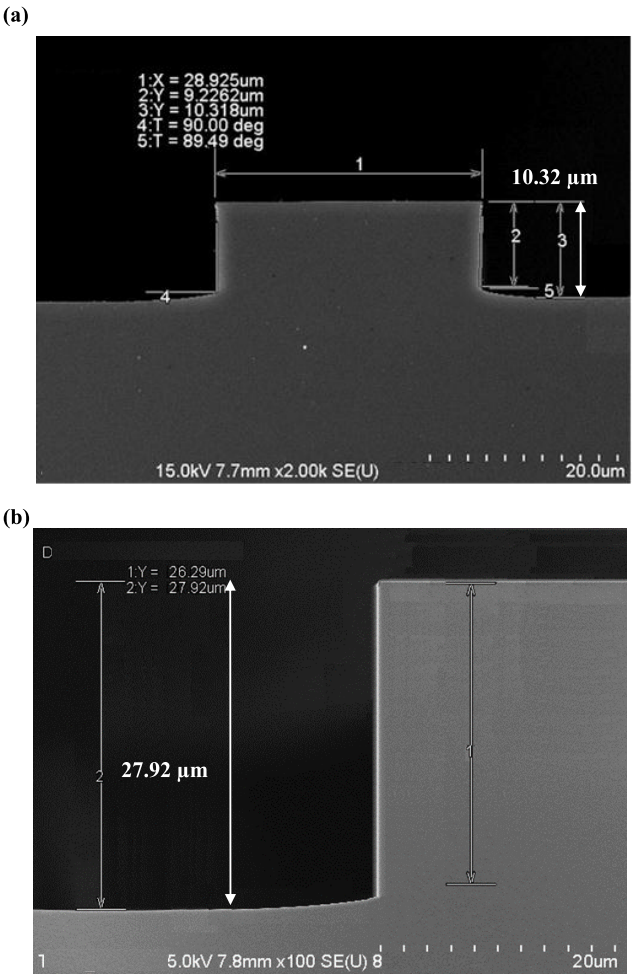


Figure 5. SEM micrographs showing the cross-sections and measured depths of two cavities: (a) the cavity of 10.3 μm depth, and; (b) the cavity of 27.9 μm depth.

of modulating the pressure of the sealed chamber using the etching cavities on a substrate is reported [20]. This approach could not be easily adopted on MEMS devices with a CMOS chip underneath; for example, the sensors implemented using the TSMC Si-above-CMOS platform [3]. Moreover, a few additional processes are required to fabricate the cavities. Thus, the process yield and cost and the chip size are the concerns when assessing manufacturing feasibility [20]. Thus, this study extends the concept in [21], to develop the fabrication and WLC processes to offer various sealed chamber pressures for different MEMS devices on the same wafer. In short, the hermetic chamber pressure is modulated by varying the cavity depth of the capped Si wafer. The presented approach offers various chamber pressures and could also be implemented on the foundry available Si-above-CMOS platform. In application, this study has demonstrated the presented technology by using the TSMC Si-above-CMOS platform [3].

2. Design concept

This study presents the WLC process to achieve sealed chambers with different vacuum levels by varying the cavity depth of Si capping (i.e. the chamber volume), as shown in figure 1. The wafer bonding process could specify the vacuum level of the sealed chamber, to meet the requirements for different MEMS applications. The final vacuum level is determined by the total number of gas molecules inside the sealed chamber. As reported in [22, 23], outgassing of deposited films on bonded substrates will increase the number of gas molecules inside the sealed chamber and further influence the vacuum level. In addition, the materials of thin films [22, 23] and the bonding temperature [9] will influence the number of outgassing gas molecules. According to the measurements from a residue gas analyzer, the CMOS and Si capping substrates exhibit higher percentages of hydrogen gas outgassing after baking. The measurement results set out in table 1 summarize the hydrogen outgassing from the CMOS and Si capping substrates at two different baking temperature conditions (these are the bonding temperatures for the WLC process). It indicates that the hydrogen outgassing from the CMOS substrate is nearly 10 times higher than that from Si substrates. Moreover, the Si capping substrates with different cavity depths have the same hydrogen outgassing. This study exploits the outgassing characteristic of a CMOS chip to fabricate chambers of various pressures after the WLC of the Si-above-CMOS

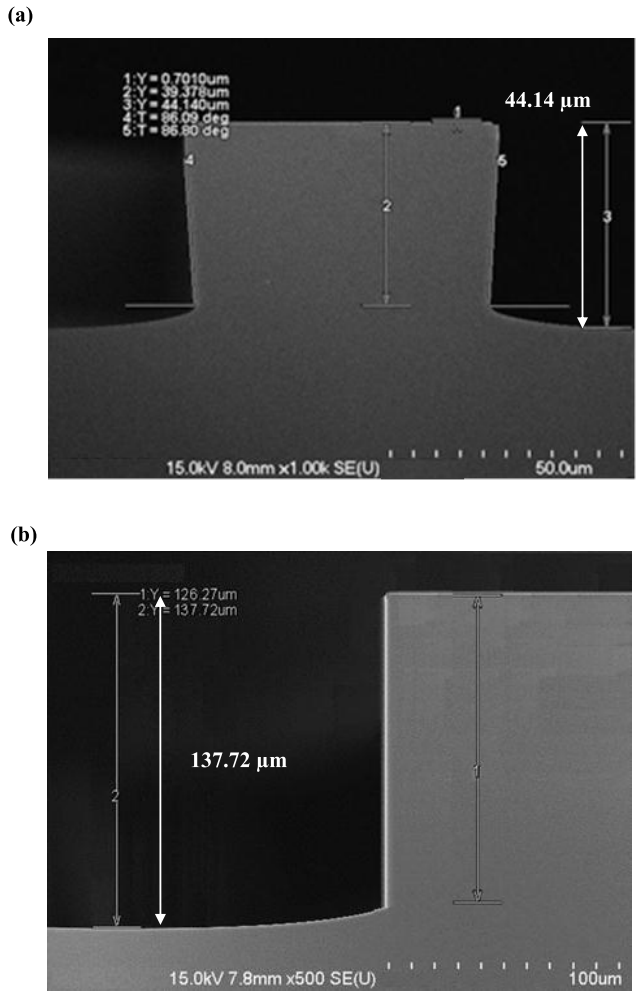


Figure 6. SEM micrographs showing the cross-sections and measured depths of two cavities: (a) the cavity of 44.1 μm depth, and; (b) the cavity of 137.6 μm depth.

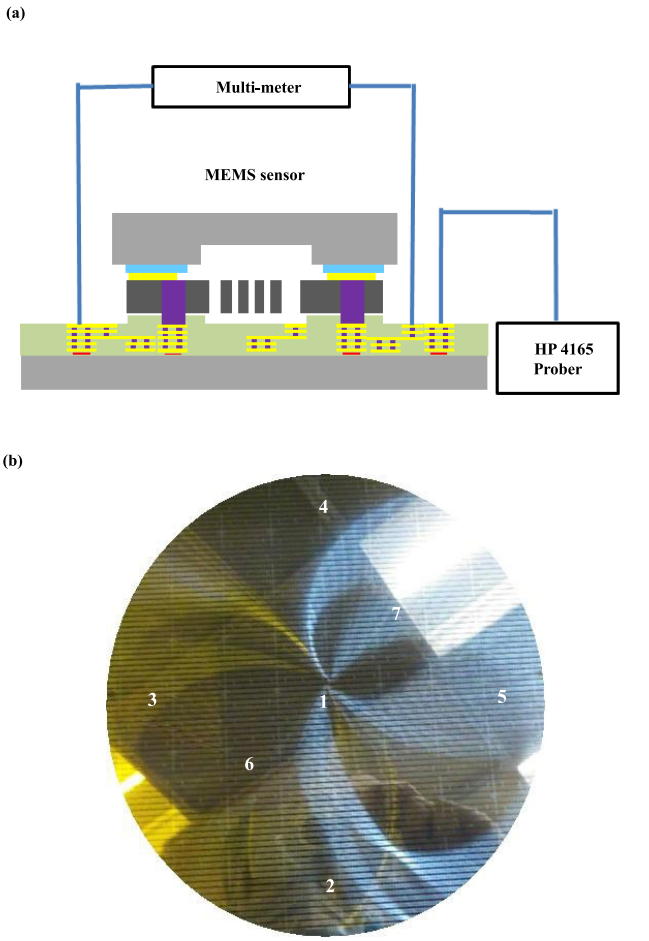


Figure 7. (a) Schematic of the test setup to measure the pressure of the sealed chamber using the embedded Pirani gauge. The metal layers and tungsten vias of the CMOS chip are employed to transmit the driving and sensing signals. (b) Photograph of a typical fabricated eight-inch wafer. The number marked on the wafer shows the seven regions (the center, edge, and in between regions) for measurement, to establish the correlated pressure distribution map.

MEMS process platform. The pressure of the sealed chamber can be modulated by chamber volume after the outgassing. Thus, various chamber pressures can be achieved for different MEMS devices fabricated and sealed on the same wafer. This study exploits the foundry available micromachining process technology, the TSMC Si-above-CMOS (0.18 μm 1P5M CMOS process) MEMS process platform, to demonstrate the presented concept. In application, the MEMS Pirani vacuum gauge with comb structures is designed and implemented using the process. By characterizing the pressure of the sealed chambers using the Pirani gauge, the proposed design concept is demonstrated.

As shown in figure 1, two MEMS devices of identical design are sealed in chambers of different volumes. Since the two MEMS devices have an identical design as well as footprint, the sealed chambers have the same amount of outgassing ideally. According to the ideal gas equation for a hermitic sealed chamber of volume V, the pressure P can be expressed as [24]

$$P = nRT/V \tag{1}$$

where n is the quantity of residue gas molecules in the hermitic sealed chamber, R is the ideal gas constant, and T is the chamber temperature. As the number of outgassing molecules is the same for the sealed chambers in figure 1, the residue gas molecules n inside these two chambers is a constant. According to equation (1), the chamber pressure P can be modulated by varying the volume V of the hermetic sealed chamber at a given temperature. This study exploits the relation in equation (1) to modulate the pressure of the hermetic sealed chamber. As indicated in figure 1, the Si-above-CMOS MEMS device is sealed by a silicon cap with cavities of different depths (i.e. D_1 and D_2). Considering the sealed Si-above-CMOS chip of the same footprint, the volume of the hermetic sealed chamber can be modulated by varying the cavity depth D_i of the silicon cap. As a result, by preparing the capping silicon wafer with cavities of different depths, various chamber pressures can be achieved for different applications after the hermetic WLP process.

3. Fabrication and results

Figure 2 shows the process flow to demonstrate the presented approach. The Si-above-CMOS process platform has been

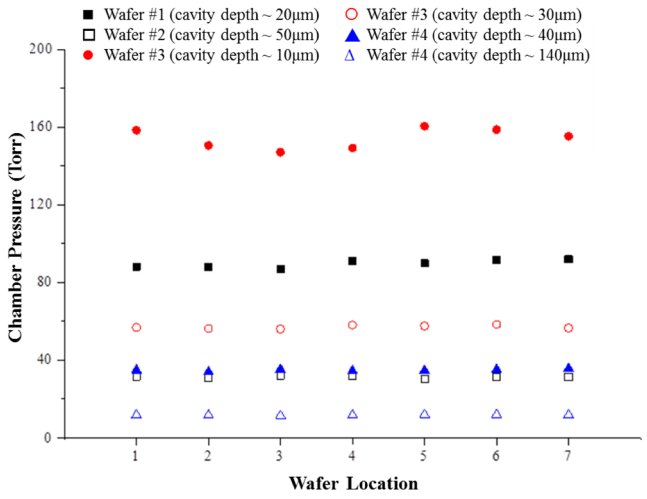


Figure 8. The pressure distribution of the seven regions measured from two wafers of different cavity depths. As denoted by (■), the cavity of 18.9 μm depth (on wafer #1) has an average chamber pressure of 89.6 Torr; as denoted by (□), the cavity of 50.5 μm depth (on wafer #2) has an average chamber pressure of 31.3 Torr; as denoted by (●), the cavity of 10.3 μm depth (on wafer #3) has an average chamber pressure of 154.2 Torr; as denoted by (○), the cavity of 27.9 μm depth (also on wafer #3) has an average chamber pressure of 57.1 Torr; as denoted by (▲), the cavity of 44.1 μm depth (on wafer #4) has an average chamber pressure of 34.9 Torr; as denoted by (△), the cavity of 137.6 μm depth (also on wafer #4) has an average chamber pressure of 11.8 Torr.

employed to implement the MEMS devices [3]. Moreover, the study further fabricates cavities of various depths on the capping silicon wafer to modulate the volume and pressure of the sealed chambers after the WLP process. As indicated in figure 2(a), the CMOS chip was prepared using the standard TSMC 0.18 μm 1P5M process. The passivation of the CMOS chip was then planarized and etched to fabricate the spacers to define the space for suspended MEMS structures. As shown in figure 2(b), a bare silicon wafer was bonded to the CMOS chip with spacers on its surface. The bonded wafer was then thinned down to the desired thickness for MEMS devices. The thickness of the thinned Si wafer was determined by the specifications of the MEMS devices. As indicated in figure 2(c), the vias were fabricated on the device silicon wafer using deep reactive ion etching (DRIE) and the tungsten deposition. The vias were employed as the electrical interconnection between MEMS devices and the CMOS chip. In addition, a metal layer was deposited and patterned on the surface of the device silicon wafer for the later bonding process. Thus, the processes for the Si-above-CMOS MEMS devices were achieved. The subsequent metal deposition and patterning processes were performed on the capping Si wafer for the following hermetic sealing. As indicated in figure 2(d), the bonding metal for the following WLC process was deposited and patterned (with a ring shape for the hermetic sealing of MEMS devices) on the Si cap. After that, the Si cap was etched to form cavities of different depths by multiple photolithography and DRIE processes. The cavity depth D_i of the capping Si wafer can be properly defined by a DRIE etching process. As shown in figure 2(e), the MEMS devices were finally encapsulated by the Si cap with cavities. Eutectic bonding was employed to meet the requirements of the hermetic seal and thermal budget.

To verify the concept presented in this study, cavities of different depths were fabricated on the capping Si wafers by using the process in figure 2(d). Thus, hermetic sealed chambers of different volumes were prepared. Moreover, in this study, the silicon based MEMS Pirani gauge [25, 26] was defined and fabricated using the process in figure 2(c). The Pirani gauge is employed for *in situ* monitoring of the pressure of the sealed chamber indicated in figure 2(e). Thus, the variation of pressure with volume for the sealed chambers is characterized.

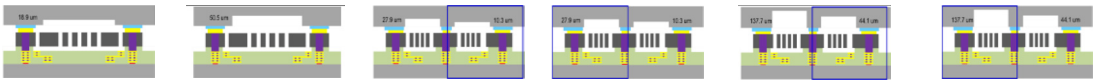
In application, this study has designed and fabricated four different types of wafers (#1 to #4) respectively sealed by Si caps with cavities of six different depths, using the process in figure 2. These four types of wafers sealed by Si caps with different cavity designs are prepared for comparison. To properly characterize the variation of pressure with volume for the sealed chambers, the Pirani gauges in each chamber have the same design and footprint. Firstly, this study fabricated two types of sealed wafers (wafers #1 and #2) having Si caps with cavities of 20 μm and 50 μm respectively. Secondly, wafer #3 was fabricated, sealed by Si caps with cavities of two different depths (10 μm and 30 μm). Finally, wafer #4 was sealed by Si caps with cavities of two different depths (40 μm and 140 μm). Thus, the variation of pressure with volume for the sealed chambers in different wafers (wafer #1 and wafer #2) is evaluated. The variation of pressure with volume for sealed chambers in the same wafer can also be evaluated using wafer #3 or wafer #4. Moreover, Si caps with cavity lengths ranging from 10 μm to 50 μm and further extending to 140 μm could offer more information about the correlation of volume and pressure for sealed chambers.

The scanning electron micrographs in figure 3 show the typical fabricated Pirani gauge embedded in each cavity for *in situ* pressure monitoring of the sealed chamber. Thus, the pressure variation with the cavity size can be characterized to validate the design concept. In addition, the micrographs in figures 4–6 show the cross-sections of cavities on Si caps defined by DRIE. Figures 4(a) and (b) respectively show the cavities on wafer #1 and wafer #2. As indicated in the micrographs, the measured cavity depths are 18.9 μm for wafer #1 and 50.5 μm for wafer #2. The etching depths have deviations of less than 6%, compared to the designed values. The micrographs in figure 5 depict cavities of two different lengths on the Si cap for wafer #3. Measurements indicate that the two cavity depths on wafer #3 are 10.3 μm and 27.9 μm. Similarly, the two cavity depths on wafer #4 measured from figure 6 are 44.1 μm and 137.7 μm.

4. Results and discussions

This study has established the test setup shown in figure 7(a) to characterize the chamber pressure through the embedded Pirani gauge. A semiconductor electrical analyzer HP4156 was connected to the bond wafer to characterize the hermetic

Table 2. Summary of the measurement results. The four wafers containing six cavities of different depths are listed. The chamber pressure, pressure ratio, and volume ratio of these cavities are also summarized.

Cavity category	Wafer1	Wafer2	Wafer3		Wafer4	
Cavity depth (μm)	20	50	10	30	40	140
SEM depth (μm)	18.9	50.5	10.3	27.9	44.1	137.7
Chamber volume ratio	1.83	4.9	1	2.71	4.28	13.37
Pressure (Torr)	89.6	31.3	154.2	57.1	34.9	11.8
Pressure ratio	1/1.72	1/4.93	1/1	1/2.70	1/4.42	1/13.07
Structure						

chamber pressure by measurement of the *I*–*V* curve. To evaluate the uniformity and distribution of the process, this study has characterized the pressure of seven hermetic sealed MEMS chambers on each wafer. The photo in figure 7(b) shows an eight-inch wafer after the fabrication process shown in figure 2. As indicated by the number in figure 7(b), the seven hermetic MEMS chambers characterized in this study are respectively located at the wafer center, at the edges, and in between. The measurement results in figure 8 show the pressure of the sealed chambers with cavity depth $D = 18.9$ μm on wafer #1 (denoted by solid square dots) and the pressure of the sealed chambers with cavity depth $D = 50.5$ μm on wafer #2 (denoted by hollow square dots). The results also depict the pressure distribution for chambers at the seven locations marked in figure 7(b). Thus, the mean chamber pressures are 89.6 Torr (for the cavities on wafer #1 with $D = 18.9$ μm), and 31.3 Torr (for the cavities on wafer #2 with $D = 50.5$ μm). The standard deviation of chamber pressure for the $D = 18.9$ μm cavity is 2.0 Torr (2.2%, when normalized to the mean chamber pressure of 89.6 Torr), and for the $D = 50.5$ μm cavity it is 0.5 Torr (1.6%, when normalized to the mean chamber pressure of 31.3 Torr).

The measurement results in figure 8 also indicate the pressure of two different sealed chambers in wafer #3. Note that the cavity depths of these two chambers (fabricated on the same Si cap) are respectively $D = 10.3$ μm (denoted by solid circular dots) and $D = 27.9$ μm (denoted by hollow circular dots). The pressure distribution for chambers at the seven different locations is also available. The mean chamber pressures detected by the embedded fabricated Pirani gauge are respectively 154.2 Torr (for the chamber with a cavity depth of 10.3 μm), and 57.1 Torr (for the chamber with a cavity depth of 27.9 μm). The standard deviation of the chamber pressure for the $D = 10.3$ μm cavity is 5.3 Torr (3.4%, when normalized to the mean chamber pressure of 154.2 Torr), and for the $D = 27.9$ μm cavity it is 0.9 Torr (1.6%, when normalized to the mean chamber pressure of 57.1 Torr). Moreover, the measurement results in figure 8 indicate the pressures of the two different sealed chambers in wafer #4. The mean chamber pressures are 34.9 Torr (for the chamber of $D = 44.1$ μm, as denoted by solid triangular dots), and 11.8 Torr (for the chamber of $D = 137.7$ μm, as denoted by hollow triangular dots). The standard deviation of the chamber pressure for the $D = 44.1$ μm cavity is 0.6 Torr (1.7%, when normalized to the mean chamber pressure of 34.9 Torr), and for the $D = 137.7$ μm cavity it is 0.2 Torr (1.7%, when normalized to the mean chamber pressure of 11.8 Torr). Thus, the measurement results show high confidence levels. Table 2 summarizes the fabrication and measurement results to indicate the correlation between the volume and the pressure of the sealed chambers. The results indicate that the chamber volume is easily modulated by the cavity depth *D*. In this study, the chamber volume could be increased 13.3-fold as the cavity depth increased from 10.3 μm to 137.7 μm. Moreover, measurement results further indicate that the chamber pressure dropped to only 1/13.1 as the cavity depth increased from 10.3 μm to 137.7 μm. Similarly, other results in table 2 also agree well with the relation between the hermetic chamber pressure and the cavity depth in equation (1), $PV =$ constant. Since the footprint of each chamber is the same, the relation could be expressed as $PD =$ constant. Figure 9 further shows the correlation of the pressure and $1/D$ for the six sealed chambers with different depths. It indicates that the hermetic chamber pressures of all six chambers are proportional to $1/D$. The results agree well with the prediction from the presented concept. In short, the modulation of sealed chamber pressure after the WLC process can be achieved by varying the cavity depth of the capping Si wafer.

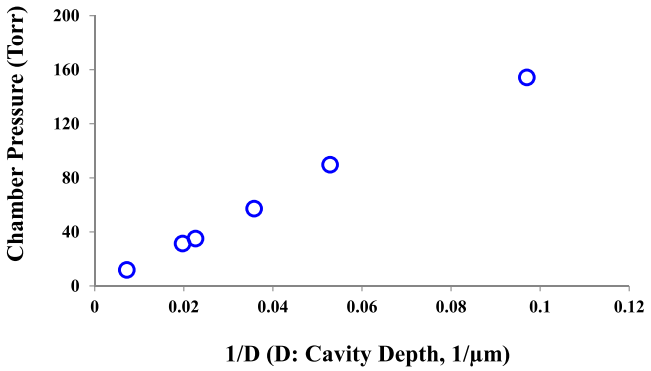


Figure 9. The correlation of the average measured pressure and $1/D$ for the six sealed chambers with different cavity depths.

5. Conclusions

When compared with SiP technology, there are many advantages in using the SoC solution. Thus, various process platforms have been developed to monolithically fabricate and integrate different MEMS devices on a single chip. Moreover, the WLC process is used to further seal and protect the

suspended MEMS devices after fabrication. The encapsulated MEMS devices have various chamber pressure requirements for different applications, such as accelerometer and gyroscope. It is crucial to realize sealed chambers of different ambient pressures using the WLC process for the SoC solution. This study presents the concept to modulate the ambient pressure of an encapsulated MEMS device by varying the volume of the sealed chamber. The outgassing of oxide film is exploited as the pressure source. The volume of the sealed chamber is easily controlled by the cavity depth D of the Si capping wafer, using the DRIE process. To demonstrate the concept of the presented approach, the foundry available process (TSMC's Si-above-CMOS MEMS process platform) is employed to fabricate devices which are further sealed in cavities of different depths by WLC process to modulate the ambient pressure. The MEMS Pirani vacuum gauge is fabricated and encapsulated in each sealed chamber to monitor the chamber pressure. Chambers having six different cavity depths ranging from 10.3 μm to 137.7 μm are fabricated on eight-inch wafers. The chambers have the same footprint. As a result, the chamber pressures are modulated from 154.2 Torr to 11.8 Torr. Measurements show that the sealed chamber pressure is proportional to $1/D$, and a large pressure range can be modulated. The results agree well with the prediction from this study, and the feasibility of this simple chamber pressure modulation approach on an eight-inch wafer is also demonstrated. In conclusion, the ambient pressures for the operation of an accelerometer and a gyroscope have a near 10-fold difference [9]. Thus, the presented approach enables the formation of sealed chambers with vacuum levels ranging from 11.8 Torr to 154.2 Torr to meet the operation pressure requirements for both accelerometer and gyroscope. Thus, the accelerometer and gyroscope can be monolithically fabricated using the TSMC Si-above-CMOS platform [3] and then WLC packaged using the presented approach to achieve a six-axis inertia sensing unit.

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