Monolithic CMOS—MEMS Pure Oxide Tri-Axis Accelerometers for Temperature Stabilization and Performance Enhancement

Ming-Han Tsai, Yu-Chia Liu, Kai-Chih Liang, and Weileun Fang, *Fellow, IEEE*

***Abstract*— A complementary metal–oxide–semiconductor (CMOS)–microelectromechanical system (MEMS) accelerometer with stacked pure oxide layers as mechanical structures was developed. Metal layers were confined to the sensing electrodes and electrical routings; the metal–oxide composite in the CMOS–MEMS accelerometer was distributed in limited regions. This design has two major advantages: 1) the thermal deformation of suspended MEMS structures resulting from a mismatch in the coefficients of thermal expansion of the metal and the oxide in the metal–oxide films is suppressed; and 2) the parasitic capacitance of the sensing electrode routing underneath the proof mass is reduced. Thus, the accelerometer has higher sensitivity and reduced thermal drift. The curvature of the mechanical structures are improved in the temperature span and the noise floor is lowered. In the full temperature span (30 °C–90 °C), change in the radius of curvature per unit change in the temperature was 0.08%/°C for the in-plane accelerometer and 0.37%/°C for the out-of-plane accelerometer. Compared with the typical metal–oxide design, the proposed pure oxide design yielded a >20-fold improvement in radius of curvature change per unit temperature change for the in-plane accelerometer and a fivefold improvement for the out-of-plane accelerometer. Moreover, the noise floor was reduced to 0.40 (x-axis), 0.21 (y-axis), and 0.94 mG Hz$^{-1/2}$ (z-axis), respectively, a 2.2–7.6-fold improvement compared with the metal–oxide design. [2015-0012]**

***Index Terms*— Complementary metal oxide semiconductor–microelectromechanical system CMOS–MEMS, tri-axis accelerometers, pure oxide structure, coefficient of thermal expansion (CTE) mismatch, parasitic capacitance.**

I. INTRODUCTION

IN ADDITION to industrial and automobile applications, microelectromechanical system (MEMS) inertial sensors, such as accelerometers and gyroscopes, have been widely used in such applications as portable and medical electronics. Miniaturization is crucial in MEMS accelerometers for both cost saving and increased integration [1], and various fabrication approaches, such as bulk and surface micromachining, have been developed to meet these requirements [2]–[4]. In addition, the complementary metal oxide semiconductor (CMOS) technique, used in many existing foundries, can be extended to realize MEMS sensors. Thus, suspended MEMS structures can be fabricated using the post-CMOS process and integrated with CMOS electronics on a single chip. This CMOS–MEMS technology is considered a promising single-chip solution for fabricating various high-performance sensors, such as inertial sensors [5], microphones [6], chemical sensors [7], and radio frequency-MEMS devices [8], [9]. Moreover, the CMOS–MEMS technology enables zero-level packaging [10].

For CMOS–MEMS applications, metal/SiO_2 layers are stacked not only for providing electrical routing and insulation but also for fabricating the MEMS structure. A CMOS–MEMS structure composed of multiple metal–dielectric layers is usually deformed by thin film residual stresses after the film is released from the substrate [11]. The released CMOS Al film exhibits stress relaxation because it is subjected to many thermal processes from chip packaging to IC soldering [12]. Thus, the extensive use of metal films in the structure may affect their reliability. Moreover, the coefficient of thermal expansion (CTE) mismatch in metal–oxide films introduces structural deformation when the temperature changes. This deformation is severe in large CMOS–MEMS accelerometers [13]. Therefore, appropriate structural design is crucial for CMOS–MEMS accelerometers. To date, several approaches for improving the structure design have been reported [14]–[18]. Polysilicon has been used as a heater to introduce a thermal load to overcome residual stress; however, high power consumption (nearly 100 mW) and a band-gap reference circuit design are required to prevent the thermal deformation [14]. Post-CMOS processes have been developed in [15] and [16] to realize thick and stiff silicon substrates that prevent the bending of CMOS–MEMS structures; however, such design entails complicated double-sided deep reactive ion etching and necessitates control over the time-dependent etching process. The integration of nickel blocks with CMOS–MEMS structures improves the sensitivity and noise performance of the fabricated sensors [17], but additional seed layers and an

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M.-H. Tsai is with PixArt Imaging Inc., Hsinchu 30013, Taiwan (e-mail: penny_tsai@pixart.com).

Y.-C. Liu is with the Institute of NanoEngineering and MicroSystems, National Tsing Hua University, Hsinchu 30013, Taiwan (e-mail: s9835804@m98.nthu.edu.tw).

K.-C. Liang is with the Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan (e-mail: s101033807@m101.nthu.edu.tw).

W. Fang is with the Institute of NanoEngineering and MicroSystems, National Tsing Hua University, Hsinchu 30013, Taiwan, and also with the Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan (e-mail: fang@pme.nthu.edu.tw).

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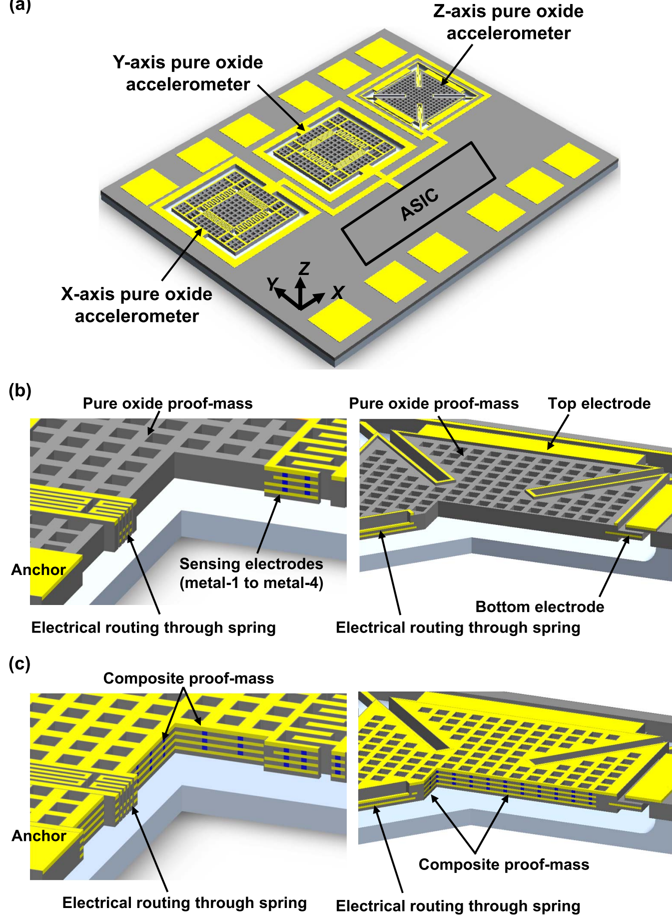


Fig. 1. (a) Perspective-view schematic of three individual accelerometers integrated with a multichannel readout circuit, (b) the proposed design (stacked pure oxide layers), and (c) existing design (stacked metal/via/oxide composite films).

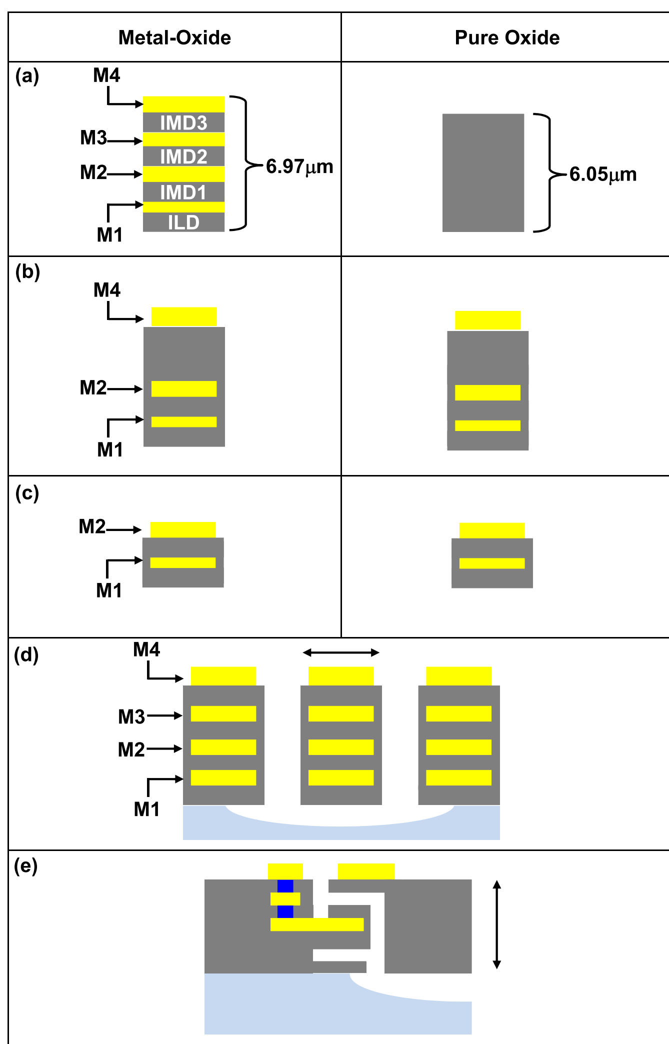


Fig. 2. Cross-sections showing the stacking of metal and oxide films for (a) the proof mass, (b) in-plane spring, (c) out-of-plane spring, (d) in-plane electrodes, and (e) out-of-plane electrodes.

electroplating process are required. The use of the symmetrical layer stacked design to balance the stress caused by temperature change was investigated in [18]. However, fully differential sensing is not available because of the limited electrical routings.

To overcome the aforementioned problems, this study extended the design concept of [19] to develop tri-axis capacitive CMOS–MEMS accelerometers. The structure is designed and implemented using the standard Taiwan Semiconductor Manufacture Company (TSMC) 0.35-μm 2P4M process and in-house post-CMOS processing. The suspended MEMS structure mainly consisted of pure oxide material, and metal layers were used only for capacitance sensing and electrical routing. Thus, the metal–oxide composite was confined to the capacitive sensing electrodes and routing wires, unlike in existing CMOS–MEMS accelerometers [11], [13], [14]. Consequently, the CMOS–MEMS accelerometer developed in this study has several unique features. In particular, thermal deformation of suspended MEMS structures resulting from CTE mismatch in metal–oxide films was suppressed. In addition, the parasitic capacitance of the sensing electrode routing underneath the proof mass decreased. The proposed concept of pure oxide structures can also be applied to other CMOS–MEMS sensors.

II. Tri-Axis Accelerometers and Circuit Design

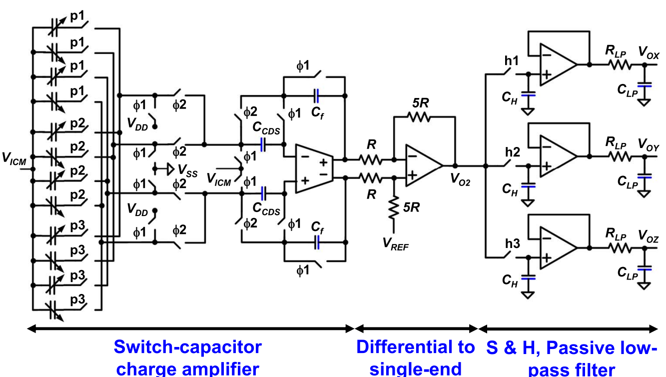
Fig. 1 is a schematic of the chip design for the proposed tri-axis accelerometer. The chip consists of three sensing units employed to detect the tri-axis accelerations (Fig. 1a). These three sensing units together with the analog circuit used for motion signal detection were monolithically integrated on a chip. The MEMS structure design was based on the standard TSMC 0.35-μm 2P4M process. Thus, the spring, proof mass, sensing electrodes, and stress compensation frame of the developed accelerometers were formed using metal and dielectric layers and the standard CMOS process. Fig. 1b illustrates the proposed design concept for improving the CMOS–MEMS accelerometer. In this design, metal layers were utilized only in the sensing electrodes and the fully differential electrical routings used for establishing circuit connections. The typical design of existing CMOS–MEMS accelerometers is illustrated in Fig. 1c for comparison, and Fig. 2 depicts the layer stacking for the spring, proof mass, and sensing electrodes of the sensors shown in Figs. 1b and 1c. As depicted in Fig. 2a, the suspended structures, such as proof

TABLE I
CMOS–MEMS TRI-AXIS ACCELEROMETER DESIGN SPECIFICATIONS

Design and simulation specification of the 3-axis sensing element		
	X & Y-axis Pure oxide/Metal oxide	Z-axis Pure oxide/Metal oxide
MEMS size	425μm × 515μm	485μm × 485μm
Proof-mass size	255μm × 420μm	410μm × 410μm
Thickness of proof-mass	6.05/6.97 μm	6.05/6.97 μm
Thickness of spring	6.97 μm	3.41μm
Spring stiffness (k)	3.95N/m	2.25N/m
Resonance frequency (f_n)	9.21/5.12 KHz	6.04/3.56 KHz
Weight of proof-mass (m)	1.18/3.81 μgram	1.56/4.48 μgram
Initial sensing capacitance (C_s)	337.2fF	272.8fF
Capacitance change with acc. (ΔC/G)	3.66/11.82 fF/G	6.94/19.93fF/G
Parasitic capacitance estimation (C_p)	279.1fF/415.7fF	283.5fF/549.3fF
Circuit Noise Equivalent Acc. (CNEA)	10.16 μG $Hz^{-1/2}$	10.16 μG $Hz^{-1/2}$
Brownian Noise Equivalent Acc. (BNEA)	0.18 mG $Hz^{-1/2}$	0.2 mG $Hz^{-1/2}$
Total Noise Equivalent Acc. (TNEA)	0.18 mG $Hz^{-1/2}$	0.2 mG $Hz^{-1/2}$

mass and stress compensation frame, are mainly composed of pure oxide. As shown in Figs. 2b and 2c, the electrical routing is distributed in springs to transmit sensed signals from the suspended structures to a circuit. Hence, in addition to pure oxide layers, the in-plane folded springs were composed of Metal-1, Metal-2, and Metal-4 films, and the out-of-plane springs were composed of Metal-1 and Metal-2 films. As indicated in Fig. 2d, the in-plane sensing electrodes contained all four metal layers (Metal-1 to Metal-4), the interlayer dielectric (ILD) layer, and four intermetal dielectric (IMD1–IMD4) layers as protection materials. The top electrode of the z-axis accelerometer comprised Metal-4 and IMD3 layers (Fig. 2e). The bottom electrodes consisted of Metal-2 as the conductor, which was surrounded by insulation layers (IMD1 and IMD2) for wet-etching protection. Metal-1 and Metal-3 films served as the sacrificial layers; therefore, the large-area bottom sensing electrodes were suspended using metal wet etching. Moreover, the out-of-plane sensing gap is defined by the thickness of the Metal-3 layers. In general, the CTE of the metal film (Al–Cu) in the CMOS process is approximately two orders of magnitude larger than that of the dielectric layer (silicon dioxide). As temperature changes, different elongations of the metal and dielectric layers induce a bending moment. Thus, suspended MEMS structures with stacked metal oxide layers are deformed by the thermal bending moment. The proposed pure oxide structure design reduces the undesired thermal deformation caused by CTE mismatch. Table 1 presents the structural design parameters of the in-plane and out-of-plane accelerometers. Related details of the layer composition are provided in [20].

In this study, the timing-based, fully differential monolithic readout circuit for tri-axis accelerometers used an improved version of the design presented in [21]. The circuit architecture consisted of three stages (Fig. 3a). A change in the fully differential capacitance of each axis was transferred to voltage using a switched capacitor charge amplifier. The differential signal was then converted to a single-ended signal and amplified using a differential-to-single-ended amplifier. Each sensing signal was finally extracted through sample-hold circuits and a passive low-pass filter. The sequential eight-channel timing



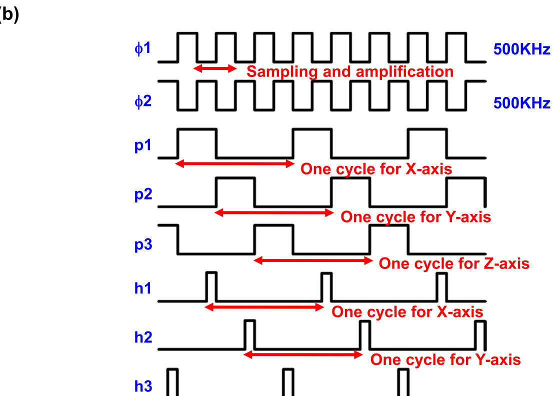


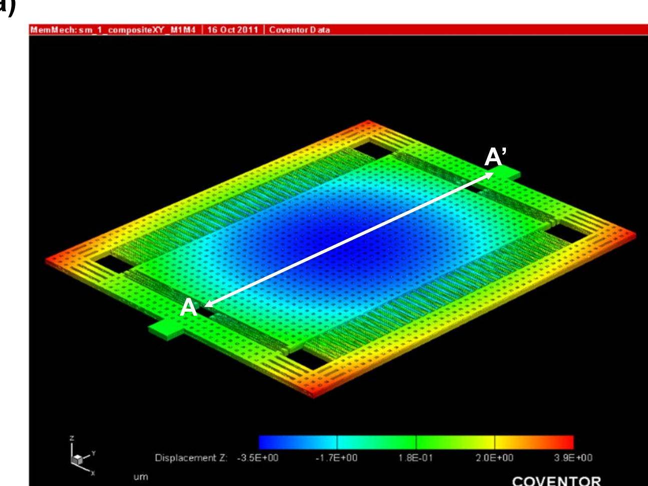
Fig. 3. (a) Schematic of the multichannel readout circuit employed for the tri-axis accelerometer used in this study, and (b) timing clocks distributed in (a).

clocks ($\phi 1$–$\phi 2$, p1–p4, and h1–h3) were precisely generated by a field-programmable gate array, as shown in Fig. 3b. The eight-channel timing clocks control the switches used for the sampling of each axis; therefore, the three-axis signals can be extracted using a single circuit to save chip area and power. The mechanical structure design and simulation issues are discussed in the following sections.

A. Thermal Deformation of MEMS Structures Caused by CTE Mismatch

This study predicted the thermal deformation caused by CTE mismatch in thin films for pure oxide and metal–oxide composite structures. The thermal deformation of a structure was predicted through finite element simulation after applying a temperature change to the finite element model, which was established on the basis of the geometry and layer stacking of accelerometers, except for the small tungsten via layers between metal layers. Moreover, the initial deformation of structures because of thin film residual stresses was considered in the model [22], [23]. The deformation of the suspended CMOS–MEMS structure was evaluated from the radius of curvature (ROC) of a test cantilever array. The test cantilevers were easily fabricated and modeled. The layer stacking of test cantilevers corresponds to that of accelerometers, for instance, stacks of pure oxide and metal–oxide layers. Moreover, layer stacking of test cantilevers was performed using standard TSMC CMOS processes, and the thicknesses of all film layers were identical for both the test cantilevers and accelerometers. Finite element models for test cantilevers of different stack layers have been established. After the initial deformations of the fabricated cantilevers were measured, the equivalent bending moment of each test cantilever was obtained from the finite element model. The equivalent initial bending moment was specified in model, which then predicted the initial bending deformation of the suspended accelerometers. Figs. 4a and 4b show typical simulation results for thermal deformations of in-plane and out-of-plane accelerometers, respectively. The ROCs of the MEMS structures were then obtained from the simulation results. The percentage change in the ROC of the proof mass of the metal–oxide accelerometer was 1.60%/°C (along AA′ in Fig. 4a) for a temperature increase of 60 °C. The deformation results from the CTE mismatch of aluminum and silicon dioxide. In the proposed pure oxide accelerometer design, the percentage change in the ROC of the proof mass (also along AA′) was reduced to only 0.07%/°C for the same amount of increase in temperature (i.e., 60 °C). In other words, the thermal deformation of the pure oxide structure was reduced by a factor of 23. Moreover, the simulations indicated that percentage changes in the ROC of the proof mass (along BB′ in Fig. 4b) for the out-of-plane accelerometer were 0.63%/°C for the pure oxide design and 1.76%/°C for the metal–oxide design for a temperature increase of 60 °C. The pure oxide design exhibited lower thermal deformation, which reduces the thermal drift. However, because of the design rules in the CMOS process, the proof mass of the pure oxide accelerometer was thinner

(a)



(b)

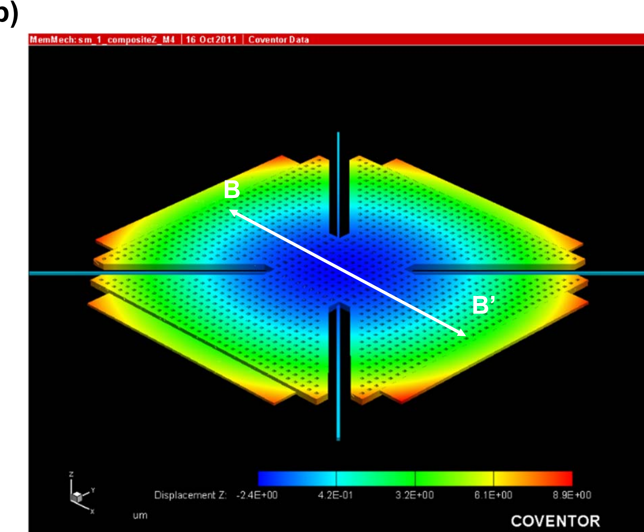


Fig. 4. Finite-element (CoventorWare) simulation results for deformation induced by CTE mismatch. Metal–oxide composite films of (a) the in-plane accelerometer and (b) the out-of-plane accelerometer.

than that of the metal–oxide accelerometer, (Fig. 2a). Thus, compared with metal–oxide accelerometers, the weight and stiffness of pure oxide accelerometers were 15.5% and 37% lower, respectively. The weight and stiffness of the proof mass of the metal–oxide accelerometer was further increased by adding tungsten vias. Specifically, the proof mass of the pure oxide accelerometer weighed 322% lesser than that of the proof mass of the metal–oxide accelerometer filled with the maximum possible tungsten vias (by following the design rules).

This study also investigated the thermal deformation about the distribution of metal–oxide areas by using finite element simulations. The thermal deformation of a suspended proof mass is related to the area occupied by the stacked metal and oxide layers (i.e., the sensing electrodes). Three simulation models with different metal areas were established to quantify the effect. These three models were characterized by 1) a proof mass which metal layers were distributed only in the sensing electrodes (Fig. 1b), 2) all structures being metal–oxide

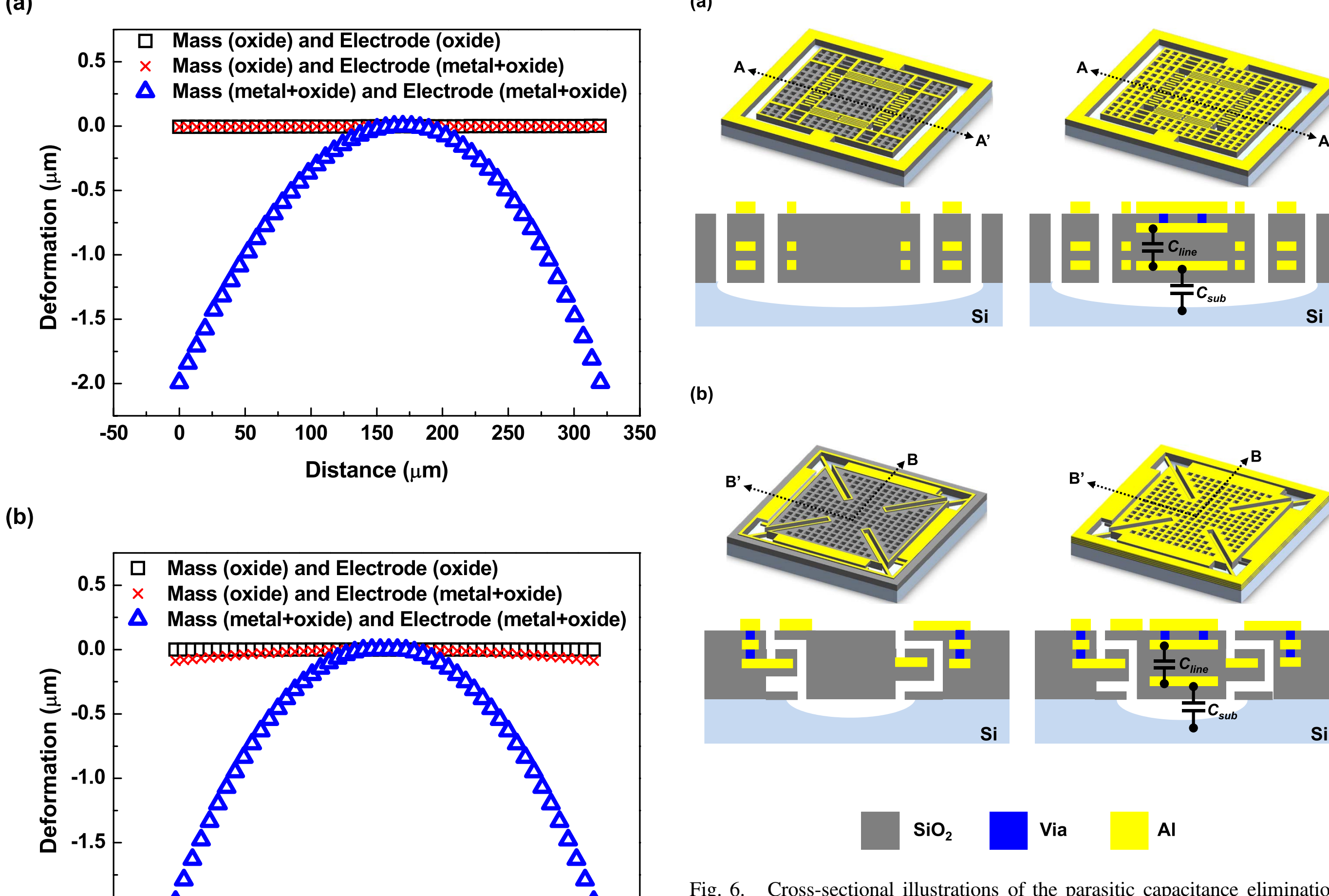


Fig. 5. Finite-element (CoventorWare) simulation results used for quantifying the thermal deformation introduced by the metal–oxide layer stacks distributed in different regions: (a) in-plane accelerometer and (b) out-of-plane accelerometer.

Fig. 6. Cross-sectional illustrations of the parasitic capacitance elimination for the pure oxide stack for (a) in-plane accelerometer and (b) out-of-plane accelerometer.

structures (Fig. 1c), and 3) all structures being oxide structures. The thermal deformations of the proof masses of the in-plane and out-of-plane accelerometers for a temperature increase of 60 °C predicted by these three simulation models are shown in Fig. 5. No thermal deformation occurred for pure oxide proof masses and very small thermal deformations were induced by the metal layers in the electrodes. However, the model with only metal–oxide proof masses exhibited large thermal deformations. These results indicated the effect of the area of the metal–oxide structure on thermal deformation. In summary, unlike in metal–oxide structures, thermal deformation caused by CTE mismatch was suppressed in pure oxide structures.

B. Parasitic Capacitance

Fig. 6 shows the details of the concept proposed to eliminate parasitic capacitance (C_p) using pure oxide structures. Fig. 6a presents the cross-sections of the proposed (left) and the existing (right) in-plane accelerometers. The existing design with composite metal–dielectric layers induces a parasitic capacitance C_{line} between the metal electrical routings and another parasitic capacitance C_{sub} between the electrical routing and the silicon substrate. By contrast, the proposed design using pure oxide structure shows reduced C_{line} and C_{sub} because of the absence of metal layers. Thus, the total parasitic capacitance C_p of the proposed design was substantially reduced. Moreover, the mechanical sensitivity (S_{mech}) of the capacitive accelerometer was improved [5]. The expression for S_{mech} can be written as

$$S_{mech} \propto \frac{4C_s}{C_P + 2C_s} \tag{1}$$

where C_s is the initial sensing capacitance of the accelerometer. Similarly, C_p for the out-of-plane accelerometer was reduced by the proposed design, as depicted in Fig. 6b. As shown in Table 1, the estimated parasitic capacitances of the proposed accelerometers were 279.1 (in plane) and 283.5 fF (out of plane). In comparison, the parasitic capacitances of the accelerometers in Fig. 1c (with the same dimensions listed in Table 1) were estimated to be 415.7 (in plane) and 549.3 fF (out of plane). For the accelerometer with metal–oxide stacked layers, C_p increased with the size of the proof mass. The simulated circuit noise and calculated Brownian noise are listed in Table 1. The total noise was dominated by the Brownian noise.

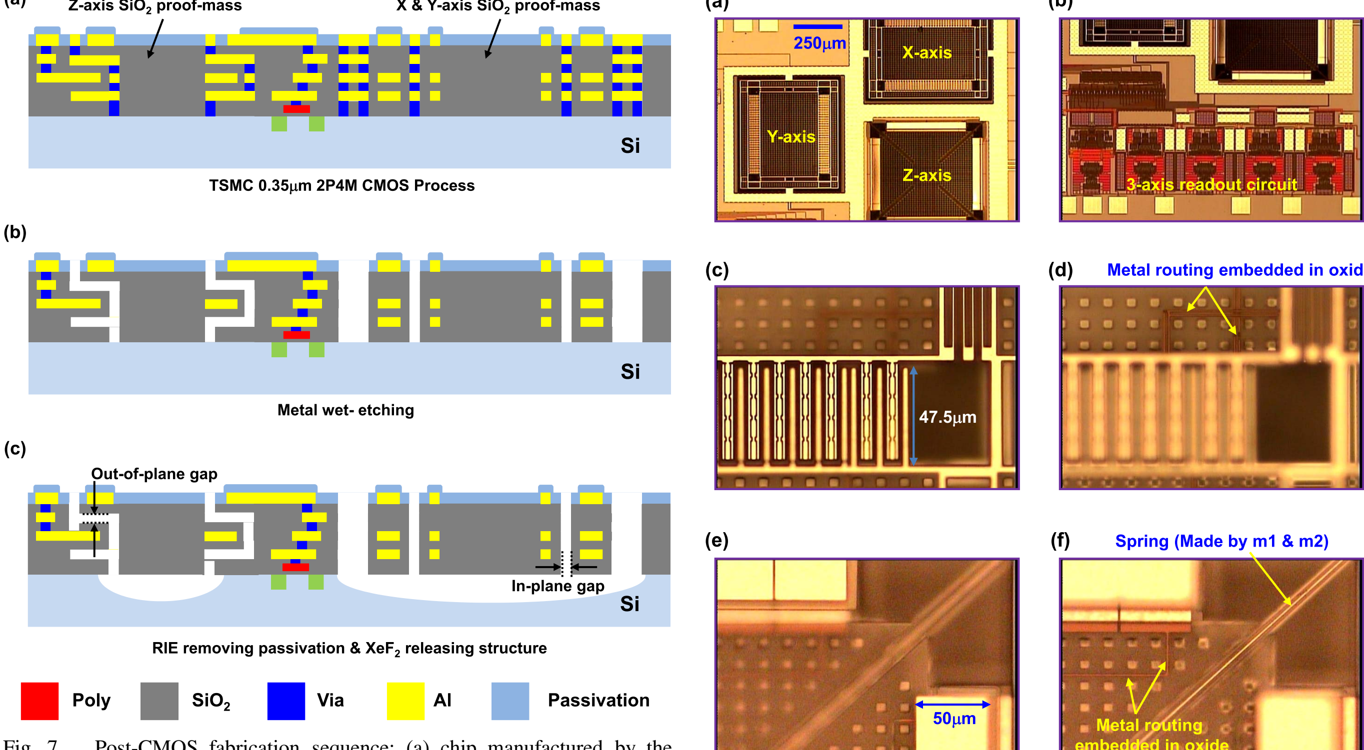


Fig. 7. Post-CMOS fabrication sequence: (a) chip manufactured by the standard TSMC 0.35-μm 2P4M process, (b) metal wet etching to form an accelerometer structure and a sensing air gap, and (c) RIE dry etching using XeF_2 to open the top metal for electrical testing and for the structure released from the substrate.

Fig. 8. Optical micrographs of (a) three accelerometers integrated on a single chip and (b) the multichannel readout circuit. (c–f) Magnified views of the optical micrographs of electrodes, pure oxide proof mass, and metal wire routing underneath the transparent proof mass of the in-plane and out-of-plane accelerometers.

III. Experimental Results and Discussion

This study employed the standard TSMC 0.35-μm 2P4M CMOS process for stacking and patterning the films on a chip. Subsequently, the post-CMOS metal and silicon substrate isotropic etching processes were performed to release the MEMS structures for fabricating the tri-axis accelerometer. The performance of the fabricated tri-axis accelerometer was evaluated through measurements. The details of the fabrication and testing results are discussed in the following section.

A. Fabrication Flow and Results

The fabrication process flow is illustrated in Fig. 7. Fig. 7a shows the chip prepared using the standard TSMC 0.35-μm 2P4M CMOS process on the basis of the design proposed in this study. As shown in Fig. 7b, the post-CMOS process started with metal wet-etching using H_2SO_4 and H_2O_2 solutions. Apart from exposing the silicon for release, this process defined the planar dimensions of the MEMS structures and the in-plane and out-of-plane sensing gaps. The highest aspect ratio used in this design was 11. During etching, the passivation layer was used as the protection film to define the regions for metal wet etching. In addition, the metal films, which served as the sensing electrodes and electrical routings, along the etching paths were protected by the surrounding oxide layers. According to the design rules of the standard TSMC process, the submicrometer in-plane air gap was determined by the minimum line width of the aluminum and tungsten vias, and the submicrometer out-of-plane air gap was defined by considering the thickness of the Metal-2 layer. Subsequently, the passivation layer was removed through reactive ion etching (RIE) for wire bonding. Finally, the Si substrate was isotropically etched using XeF_2 to suspend the MEMS structure, as shown in Fig. 7c. Because no metal hard mask was required for etching, the parasitic capacitance was reduced [24].

The microimages in Figs. 8a and 8b show the monolithically integrated tri-axis accelerometers and their readout circuits. The magnified photographs in Figs. 8c–8f show the distribution of metal lines in the in-plane and out-of-plane accelerometers for the sensing electrodes and electrical routings. The metal lines embedded in the transparent oxide proof mass were clearly observed using an optical microscope. The scanning electron microscope (SEM) micrograph in Fig. 9a shows a typical fabricated tri-axis accelerometer. The die size of the accelerometer is approximately 2.72 mm^2. The magnified micrographs in Figs. 9b–9d present the sensing units for the x-, y-, and z-axis, respectively. The magnified micrographs in Figs. 9e and 9f are the focused-ion-beam (FIB) cross-sections of the sensing electrodes and proof mass. The stacked metal–oxide composite films of the electrodes and the pure oxide film of the proof mass were clearly observed. Thus, the feasibility of using pure oxide for fabricating the proof mass and stress compensation frame structures of CMOS–MEMS accelerometers was demonstrated.

B. Deformation Tests for the Accelerometer

The measurement setup depicted in Fig. 10a was used to characterize the structural deformation of the accelerometer

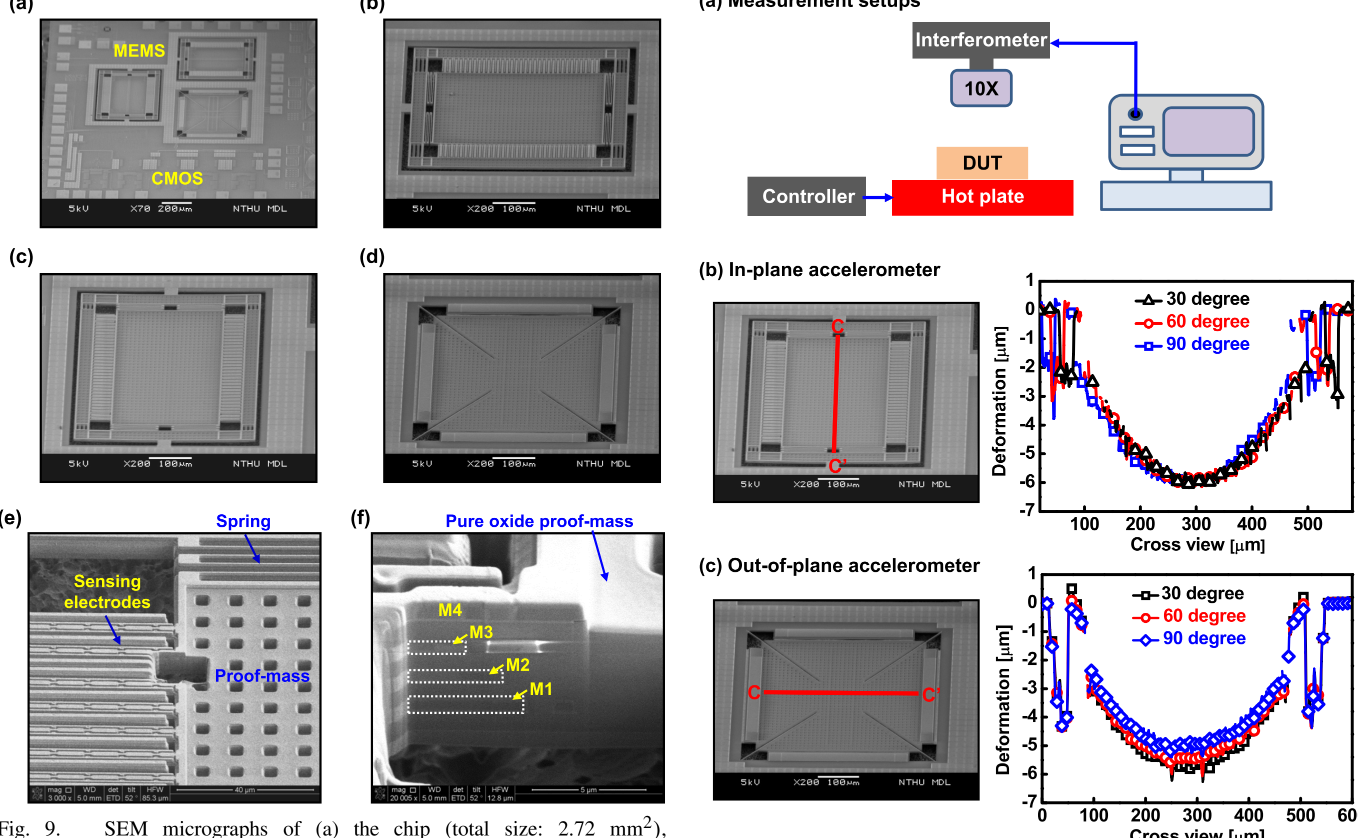
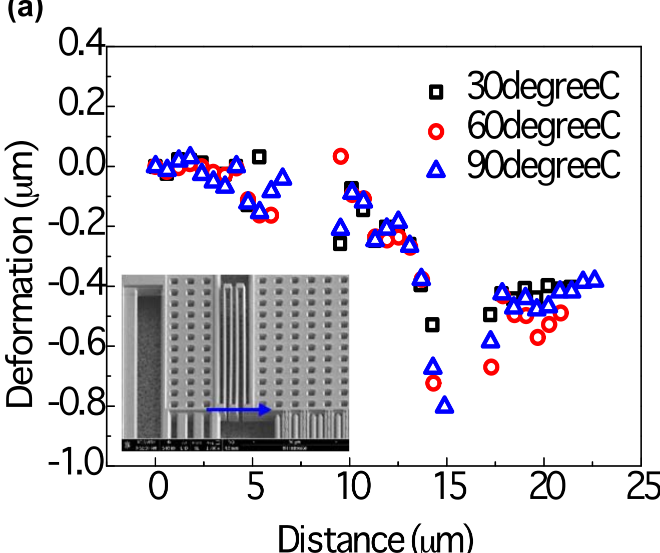


Fig. 9. SEM micrographs of (a) the chip (total size: 2.72 mm^2), (b–d) standalone x-, y-, and z-axes accelerometer structures, and (e, f) FIB cut around the sensing electrodes and proof mass to investigate the stacked film.

Fig. 10. (a) *In situ* temperature testing setup. (b, c) Measurements of deformation of pure oxide structure for different chip temperatures.

at different temperatures. The temperature was controlled using a commercial hot plate (Linkam Ltd., THMS600) with a resolution of 0.1 °C, and structural deformation was characterized using an optical interferometer (Veeco Inc., NT-1100). Figs. 10b and 10c depict the typical measured deflection profiles of the in-plane and out-of-plane accelerometers, respectively. The deflection profiles were measured along the axis CC′ (Fig. 10b), and the measurements were performed at temperatures ranging from room temperature (30 °C) to 90 °C.

The measurement results in Figs. 10b and 10c indicate that the initial ROC of the pure oxide proof mass (at approximately 30 °C) was 4.82 mm for the x-axis in-plane accelerometer and 5.09 mm for the z-axis out-of-plane accelerometer. In comparison, the initial ROC of the metal–oxide proof mass was 7.02 mm for the in-plane accelerometer and 5.50 mm for the out-of-plane accelerometer. The chip with the tri-axis accelerometer was then heated using the hot plate to specific temperatures. The increasing temperature induced structural deformation mainly through CTE mismatch of the stacked films. With increase in the temperature from 30 °C to 90 °C, the ROC of the proof mass for the x-axis pure oxide accelerometer varied from 4.82 to 5.05 mm (i.e., percentage change in the ROC for a unit temperature change, ΔROC%/ΔT, was 0.08%/°C). Moreover, the ROC of the proof mass of the z-axis (out of plane) pure oxide accelerometer increased from 5.09 to 6.22 mm (i.e., ΔROC%/ΔT was 0.37%/°C). In comparison, for the metal–oxide accelerometers shown in Fig. 1c, with increase in the temperature from 30 °C to 90 °C, ΔROC%/ΔT was 1.65%/°C (ROC increased from 7.02 to 13.95 mm) for the in-plane accelerometer, whereas for the out-of-plane accelerometer, ΔROC%/ΔT was 1.93%/°C (ROC increased from 5.50 to 11.86 mm). These measurement results accorded with the simulation results and demonstrated that the ROC changes caused by temperature variations were substantially reduced (i.e., 20-fold in the in-plane accelerometer and 5-fold in the out-of-plane accelerometer) by the proposed pure oxide structure. Thus, undesirable capacitance changes caused by the thermal deformation of structures were also reduced. Specifically, the overlap area of the sensing electrodes in the in-plane accelerometers was determined from the surface profiles measured using the optical interferometer. Compare with the ideal design, the overlap area (and sensitivity) for the pure oxide and metal–oxide designs decreased by 14.5% and 24.1%, respectively. In addition, the temperature-induced ROC change resulted in changes in the overlap area of the sensing electrodes and sensitivity. For instance, the overlap area for the pure oxide and metal–oxide designs at 80 °C reduced by 16.7% and 31.9% compared with the ideal overlap area. The out-of-plane thermal deformation is especially critical to the z-axis accelerometer because it leads to an additional gap-closing sensing capacitance change. The simulation results for the out-of-plane thermal deformation were not consistent with the measurement results, mainly because of the following two reasons. First, the material properties of the CMOS metal and oxide layers were different from those employed in the



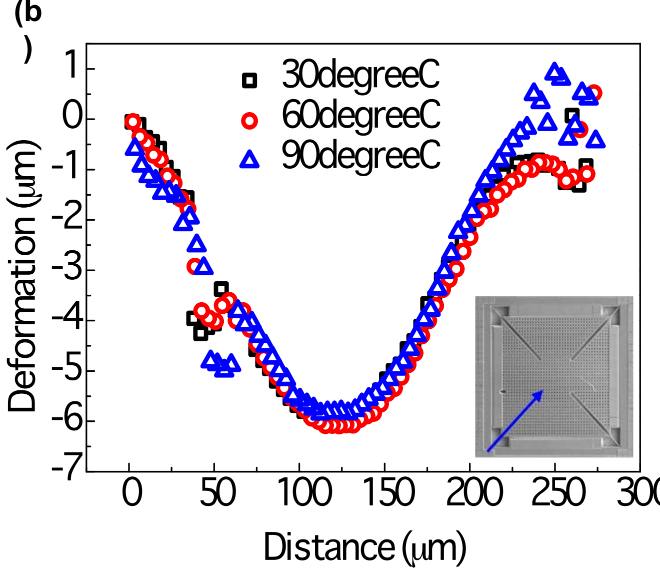


Fig. 11. Measured thermal deformation of the (a) in-plane and (b) out-of-plane springs.

simulations, because the metal layer contained a small amount of copper; furthermore, the plasma-enhanced chemical vapors deposition and tetraethyl orthosilicate oxides had different material properties. Second, according to TSMC technology files, the thickness of the oxide layer may vary by up to 20%. Moreover, the in-house post-CMOS processes, such as RIE used for removing the passivation layer, changed the thickness of the remaining oxide. Proof mass stiffness varies with the third power of its thickness. Thus, thickness variation is a major factor contributing to the discrepancy between the simulations and measurements. In summary, the results demonstrate that the pure oxide structure substantially reduces thermal deformations in CMOS–MEMS accelerometers.

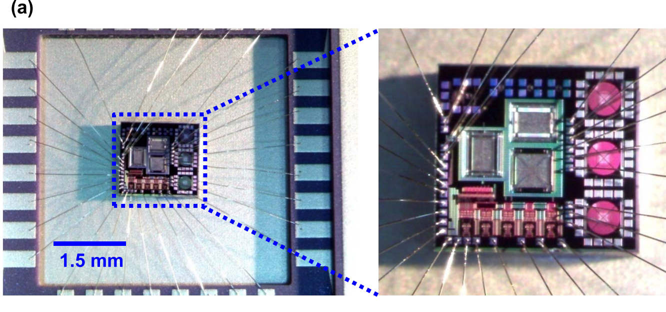
Furthermore, the out-of-plane thermal deformations of the springs were characterized using the optical interferometer, (Fig. 11). As shown in Fig. 1, the two ends of the springs (both in-plane and out-of-plane springs) were constrained by the anchor and proof mass. Because the in-plane spring was relatively thick, it was insensitive to temperature variation. Curling mainly resulted from the initial deformation caused by the thin film residual stresses. Because of the design of the fixed-fixed ends, the thinner out-of-plane spring was also insensitive to temperature variation from 30 °C to 60 °C. However, as the temperature reached 90 °C, out-of-plane deformation occurred on the movable side, possibly because of the buckling of the spring–mass–spring structure supported by the long, thin, and straight springs. Spring designs for the pure oxide and metal–oxide accelerometers were identical. The shape and layer stacking of springs can be redesigned to further reduce curling.

C. Accelerometer Performance Tests

First, the resonant frequencies of the in-plane and out-of-plane accelerometers were measured using a commercial optical stroboscope (Umech Technologies-MMA G2) and a laser Doppler vibrometer (Polytec Scanning Vibrometer PSV 300). The measured first natural frequencies were 8.78 (for the x-axis in-plane sensing unit), 8.73 (for the y-axis in-plane sensing unit), and 5.95 kHz (for the z-axis out-of-plane sensing unit). The difference in the natural frequency between the model prediction shown in Table 1 and the device measurement results are mainly attributable to the following reasons: 1) the thin film material properties employed in the finite element model were different from those used in the measurements and 2) the dimensions of the fabricated spring mass slightly differ from those used in the simulation model. This study also characterized the shift in the natural frequency with an increase in the temperature from 25 °C to 100 °C. The temperature was controlled and monitored using the commercial hot plate. The measured natural frequency shift for the x-, y-, and z-axis accelerometers were −140, −128, and −178 ppm/°C, respectively. In other words, the resonant frequency shift caused by a temperature increase in the accelerometer contributed to the increase in the mechanical sensitivity by 0.028%/°C (x-axis), 0.025%/°C (y-axis), and 0.036%/°C (z-axis).

The monolithic CMOS–MEMS chip with a size of 1.57 mm × 1.73 mm was mounted on a dual in-line package ceramic housing (Fig. 12a). The ceramic housing was placed on a printed circuit board (PCB) for performance characterization (Fig. 12b). The input amplitude and operation frequency of acceleration were controlled and set using a function generator (Agilent Inc., 33522A) and a commercial shaker (LDS Inc., V406). The experimental setup was calibrated using a commercial piezo-based accelerometer (PCB Piezotronics Inc., Model-352C44). The output signal from the accelerometer was recorded by a spectrum analyzer (Agilent Inc., 4395A). Fig. 13 shows the typical output signal of the accelerometer measured using the spectrum analyzer under a 1 G and 100 Hz shaker excitation. The measured noise floors were 0.40 (for the x-axis sensing unit), 0.21 (for the y-axis sensing unit), and 0.94 mG $Hz^{-1/2}$ (for the z-axis sensing unit). The measured noise for the metal–oxide accelerometers was 1.4 (x-axis), 1.6 (y-axis), and 2.1 mG/rtHz (z-axis). Compared with the results in Table 2, the noise of the pure oxide accelerometers was reduced by factors in the range 2.2–7.6. The resonant frequencies of the metal–oxide

(a)



(b)

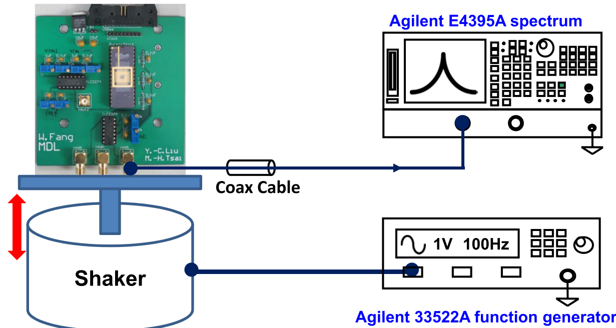
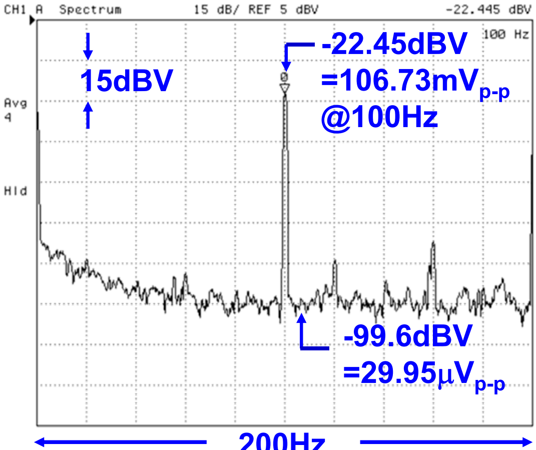
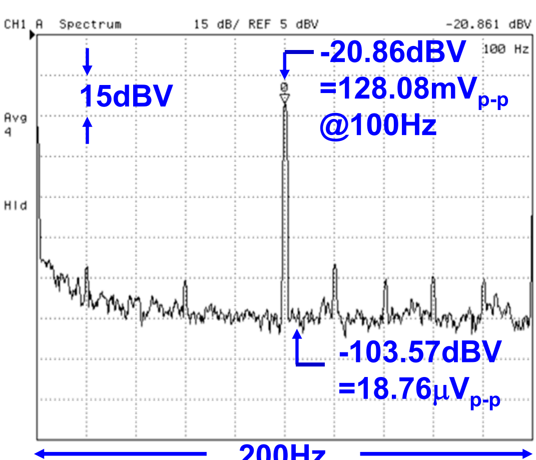


Fig. 12. (a) Tested die mounted on a ceramic housing and (b) schematic of the instruments used for the testing the CMOS–MEMS integrated circuits.

◆ X-axis output @ 1G



◆ Y-axis output @ 1G



◆ Z-axis output @ 1G

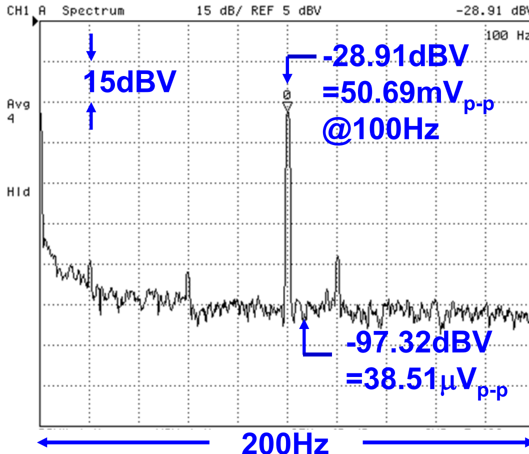


Fig. 13. Typical PCB setup and output spectra from each axis of the accelerometer after 1 G (100 Hz) shaker excitation.

composite accelerometers were 4.83 (x-axis), 4.74 (y-axis), and 3.42 kHz (z-axis). Compared with the results in Table 2, the resonant frequencies of the metal–oxide accelerometers were considerably lower. The low resonant frequencies were a result of the additional mass contributed by the Metal-4 layer and the high-density tungsten vias between the metal layers. The proof mass of the pure oxide and the metal–oxide designs differed by 322% after adding the high-density tungsten vias. The metal–oxide design with the maximum possible number of tungsten vias was employed in the measurements. Consequently, the difference in the proof mass between the pure oxide and the metal–oxide designs was 322%. The pure oxide accelerometer had higher Brownian noise [1], and its total noise was contributed to by several other sources. A major source was the parasitic capacitance in the large-area metal–oxide proof mass; the value of this capacitance was almost equal to that of the sensing capacitance. Therefore, despite the increase in the Brownian noise, the pure oxide design had low total noise. Mechanical sensitivity is proportional to the square root of the proof mass [5]. An increase in the weight of the proof mass of the metal–oxide accelerometer from 15.5% (no tungsten vias) to 322% (maximum possible number of tungsten vias) led to an increase in the sensitivity from 7.24% to 79.4%. However, although the sensitivity of the metal–oxide accelerometer increased, the total-noise-equivalent acceleration was higher than that of the pure oxide accelerometer.

Fig. 14 reveals the measured output voltages for different input accelerations. The sensitivity, nonlinearity, and cross-axis sensitivity of the accelerometers were determined. The sensitivities (nonlinearities) determined from the measurements were 105.2 mV/G (1.01%), 127.4 mV/G (0.52%), and 57.7 mV/G (2.43%) for the x-, y-, and z-axes accelerometers, respectively. The sensitivity deviation for the in-plane accelerometers (x- and y-axes sensors) of identical design was nearly 20%. The sensing gap offset is observed

TABLE II
SUMMARIZED TRI-AXIS ACCELEROMETER MEASUREMENT RESULTS

	X-axis Pure oxide/Metal oxide	Y-axis Pure oxide/Metal oxide	Z-axis Pure oxide/Metal oxide
Measurement range (G)		±2	
Frequency (kHz)	8.78/4.83	8.73/4.74	5.95/3.42
Sensitivity (mV/G)	105.2	127.4	57.7
Nonlinearity (%)	1.01	0.52	2.43
Noise floor @ 100Hz (mG $Hz^{-1/2}$)	0.4/1.4	0.21/1.6	0.94/2.1
Initial ROC at 30°C (mm)	4.82/7.08	4.98/6.82	5.09/5.5
ROC change with temperature (%/°C)	0.08/1.65	0.08/1.69	0.37/1.93
Cross-axis sensitivity X (%)		1.57	6.41
Cross-axis sensitivity Y (%)	1.05		6.07
Cross-axis sensitivity Z (%)	2.86	1.65	

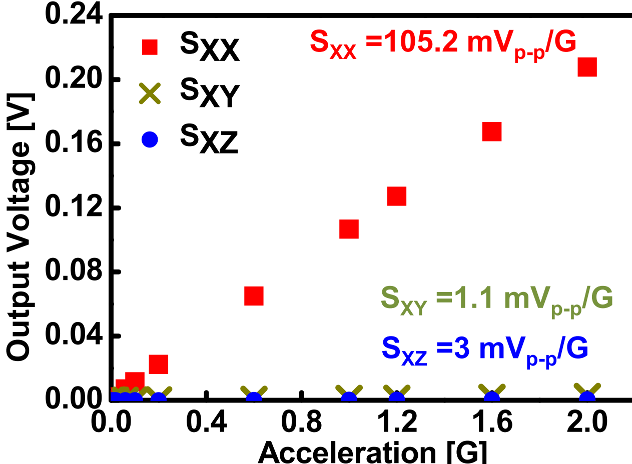
by SEM. The offset level is different between X- and Y-axis. The nonideal MEMS structure resulting from the fabrication processes was the main cause of this sensitivity deviation. For instance, the multiple metal layers in the springs may not have been perfectly aligned. Thus, the flexible springs may have had an in-plane offset d_{off} after release. The influence of the metal layer misalignment on the x-axis accelerometer was different from that on the y-axis accelerometer. In other words, the in-plane offset for the x-axis accelerometer $(d_{off})_\mathrm{x}$ differed from that for the y-axis accelerometer $(d_{off})_\mathrm{y}$. The spring offset led to an asymmetric sensing gap between the electrodes, and the total capacitance change (ΔC) can be expressed as

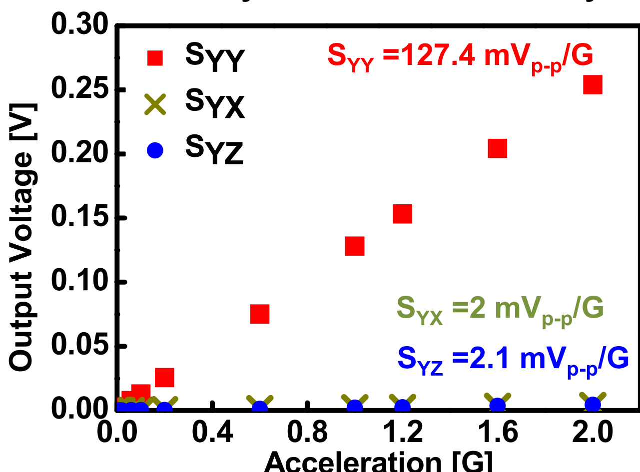
$$\Delta C = \frac{\varepsilon A}{(d - d_{off})^2}\Delta x - \frac{\varepsilon A}{(d + d_{off})^2}(-\Delta x)$$

where d is the capacitance sensing gap, d_{off} is the in-plane offset of the suspended structures, A is the overlap area, and Δx is the displacement. The difference between $(d_{off})_\mathrm{x}$ and $(d_{off})_\mathrm{y}$. resulted in different capacitance changes for the x- and y-axes accelerometers and thereby caused their sensitivities to change. Similarly, other process effects may have also caused these two sensitivities to change.

For the proposed z-axis accelerometer design, a large deformation of the proof mass caused the edges of the top and bottom electrodes to come in contact. Because the metal electrodes are surrounded by silicon dioxide, the contact will not cause a short circuit. However, the contact changes the dynamic characteristics of the z-axis accelerometer. For instance, the boundary condition and the spring stiffness of the z-axis accelerometer changes. Thus, the measured z-axis sensitivity (the value of 57.7 mV/G shown in Table2 was measured using the spectrum analyzer, and the equivalent capacitance change of the sensing electrodes was 1.82 fF/G) was much lower than the predicted value (6.49 fF/G). The structural bending caused by the residual stresses of the CMOS layers led to the poor sensitivity in the z-axis direction. This problem can be overcome using various approaches. For instance, the spring of the z-axis accelerometer should connect to the edge and not the center of the proof mass, as shown in Fig. 1. The bending deformation of the electrode and proof mass can then be suppressed [25]. The stress compensation frame concept in [26] can also be helpful for fitting the curvature of the proof mass. Moreover, the CMOS MEMS sensors implemented using the TSMC 1P6M process had considerably thick structures, which reduced the bending caused by residual stresses [25]. The maximum structure thickness was increased from 6.97 μm (for the TSMC 0.35-μm 2P4M CMOS process) to 9.31 μm (for the TSMC 0.18-μm 1P6M CMOS process). Accordingly, the bending stiffness of the proof mass can be increased by nearly 2.5 times to reduce the initial deformation induced by the thin film residual stresses. The reinforced rib design presented in [27] is another potential design that can be used to increase the stiffness of the sensing electrodes. Table 2 summarizes the measured performance of the developed tri-axis accelerometer.

Similar to [28], an aging test was performed for the CMOS–MEMS structures by using resonant excitation. The structure showed no obvious performance change after being driven for 21 billion cycles at resonance. The same testing approach was used to perform an aging test on the developed accelerometer. The accelerometer was excited using its electrostatic actuator at the resonant frequency for 200 h (6.2 billion cycles for the x- and y-axis structures and 4.1 billion cycles for the z-axis structure). The tests were performed in atmosphere (1 atm) under air-conditioning





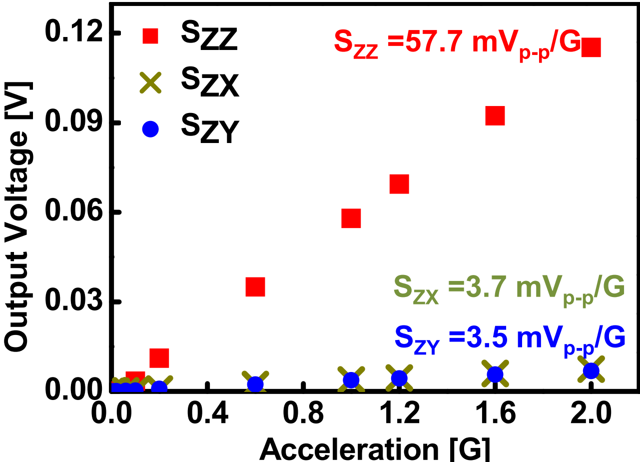


Fig. 14. Plots of typical measured output voltage and cross-axis sensitivity versus acceleration for the in-plane and out-of-plane accelerometers.

to maintain temperature and humidity at 25 °C and 45%, respectively. The frequency shift of the accelerometers after excitation was less than 20 Hz (less than 0.3% for the x-, y-, and z-axes).

IV. Conclusions

In this study, the use of stacked pure oxide layers as the main mechanical structures for a CMOS–MEMS accelerometer was proposed and successfully implemented using the standard TSMC 0.35-μm 2P4M process. The developed design has two advantages: 1) the thermal deformation of suspended MEMS structures resulting from CTE mismatch between the metal and the oxide in metal–oxide films is suppressed and 2) the parasitic capacitance of the sensing electrode routing underneath the proof mass is reduced. The thermal deformation of the proposed pure oxide in-plane and out-of-plane accelerometers improved by a factor of 20 and 5 relative to the metal–oxide design. Moreover, the noise floor improvement by a factor of 2.2–7.6 for the pure oxide design compared with the metal–oxide design. In summary, the accelerometer with a pure oxide structure exhibits enhanced performance in terms of parameters such as thermal stability, sensitivity, and noise floor compared with that fabricated using metal–oxide composites. The pure oxide structure design can be extended to other CMOS–MEMS devices, such as pressure sensors, acoustic sensors, and resonators.

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Ming-Han Tsai was born in Yunlin, Taiwan, in 1982. He received the Ph.D. degree from the Institute of NanoEngineering and MicroSystems, National Tsing Hua University, Hsinchu, Taiwan, in 2012. His research interests include microelectromechanical systems (MEMS) technology with an emphasis on CMOS-MEMS integrated sensor design, fabrication, and packaging.

He has been with PixArt Imaging Inc., Hsinchu, as a Research and Development Engineer, since 2010. He possesses several CMOS-MEMS patents in his research field. He is currently devoting himself in CMOS-MEMS-based sensors projects. His research field includes CMOS-MEMS inertial sensors, pressure sensors, and optical sensors.

Yu-Chia Liu was born in Kaohsiung, Taiwan, in 1985. He received the B.S. degree from the Department of Automatic Control Engineering, Feng Chia University, Taichung, Taiwan, in 2007, and the M.S. and Ph.D. degrees from the Institute of NanoEngineering and MicroSystems, National Tsing Hua University, Hsinchu, Taiwan, in 2009 and 2012, respectively. His Ph.D. research includes CMOS-microelectromechanical systems (MEMS) sensors developing. The related readout circuitry design is also involved.

He joined the TSMC MEMS Department, Hsinchu, in 2012, where he was an R&D Process Integration Engineer for MEMS process technology developing.

Kai-Chih Liang was born in Taipei, Taiwan, in 1979. He received the B.S. degree from the Department of Mechanical Engineering, National Chung Cheng University, Chiayi, Taiwan, in 2002, and the M.S. degree from the Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan, in 2004, where he is currently pursuing the Ph.D. degree.

He has been with the Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, since 2004, as an microelectromechanical systems (MEMS) R&D Principal Engineer for developing CMOS-MEMS platform and multiple sensors projects development into mass production. His M.S. work used the oxide wet-etching approach to realize CMOS-MEMS thermal actuator in micro hotplate application. His current research interests include CMOS-MEMS platform design for manufacturability, pressure sensor design, and multiphysics.

Weileun Fang (F'15) was born in Taipei, Taiwan. He received the Ph.D. degree from Carnegie Mellon University, in 1995. His Ph.D. research focused on the determining of the mechanical properties of thin films using micromachined structures. In 1995, he was a Postdoctoral Researcher with the Synchrotron Radiation Research Center, Taiwan. He joined the Power Mechanical Engineering Department, National Tsing Hua University, Taiwan, in 1996, where he is currently a Distinguished Professor and Member of a Faculty with the NEMS Institute. In 1999, he was with Prof. Y.-C. Tai with the California Institute of Technology, as a Visiting Associate. He has authored over 140 SCI journal papers, nearly 250 international conference papers, and 80 patents [all in microelectromechanical systems (MEMS) field]. His research interests include microelectromechanical systems (MEMS) with an emphasis on microfabrication/packaging technologies, CMOS MEMS, CNT MEMS, micro optical systems, microsensors and actuators, and characterization of thin film mechanical properties. He is the Editor-in-Chief of the *Journal of Medical Microbiology*, a Board Member of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, and an Associate Editor of the IEEE SENSORS JOURNAL and *Sensors and Actuators A*. He served as the Chief Delegate of Taiwan for the World Micromachine Summit (MMS) from 2008 to 2012, and chaired the MMS 2012. He served as the TPC of the IEEE MEMS conference, the EPC of Transducers conference, and the Regional Co-Chair and TPC Chair of the IEEE Sensors Conference. He has been a member of the International Steering Committee of Transducers since 2009. Moreover, he also serves as a Technical Consultant for many MEMS companies in Taiwan.

Dr. Fang is a Member of the Institute of Physics, U.K.