PAPER

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Determining the thermal expansion coefficient of thin films for a CMOS MEMS process using test cantilevers

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Abstract

Many standard CMOS processes, provided by existing foundries, are available. These standard CMOS processes, with stacking of various metal and dielectric layers, have been extensively applied in integrated circuits as well as micro-electromechanical systems (MEMS). It is of importance to determine the material properties of the metal and dielectric films to predict the performance and reliability of micro devices. This study employs an existing approach to determine the coefficients of thermal expansion (CTEs) of metal and dielectric films for standard CMOS processes. Test cantilevers with different stacking of metal and dielectric layers for standard CMOS processes have been designed and implemented. The CTEs of standard CMOS films can be determined from measurements of the out-of-plane thermal deformations of the test cantilevers. To demonstrate the feasibility of the present approach, thin films prepared by the Taiwan Semiconductor Manufacture Company 0.35 μm 2P4M CMOS process are characterized. Eight test cantilevers with different stacking of CMOS layers and an auxiliary Si cantilever on a SOI wafer are fabricated. The equivalent elastic moduli and CTEs of the CMOS thin films including the metal and dielectric layers are determined, respectively, from the resonant frequency and static thermal deformation of the test cantilevers. Moreover, thermal deformations of cantilevers with stacked layers different to those of the test beams have been employed to verify the measured CTEs and elastic moduli.

Keywords: coefficient of thermal expansion, elastic modulus, thin films, cantilever beam, CMOS MEMS

(Some figures may appear in colour only in the online journal)

1. Introduction

The standard CMOS process has been widely applied to fabricate micro-electromechanical system (MEMS) devices, such as accelerometers, microphones, pressure sensors, etc [1, 2]. The CMOS fabrication process for MEMS applications offers the advantage of monolithic integration of the micro mechanical structures and the integrated circuits (IC). Moreover, various mature CMOS processes are available in existing IC foundries. In many applications, the MEMS structures fabricated by such CMOS MEMS processes are stacks of metal and dielectric composite films [3–5]. Thus, the suspended MEMS structures will be deformed by the thin film residual stresses after being released from the substrate [3, 4]. Moreover, the suspended MEMS structures also frequently suffer from the unwanted deformation due to the mismatch of thermal expansion coefficients (CTEs) between the metal and dielectric films [5]. The unwanted deformation will further influence the performance and characteristics of CMOS MEMS devices. The CTE mismatch between metal and dielectric composite films has been exploited to implement a thermal actuator [6]. Therefore, CTE is one of the most important thin film mechanical properties in the standard CMOS process.

The mechanical properties of thin films are of importance in predicting the performance of MEMS devices. In general, the mechanical properties of thin films are different to those of their bulk counterparts. In addition, thin film mechanical properties also vary with film thickness, process conditions and even fabrication facilities [7–9]. Therefore, it is more reliable to directly characterize the mechanical properties of thin films fabricated using different processes such as bulk micromachining, surface micromachining and the CMOS process. Thin film mechanical properties such as Young's modulus [10], Poisson's ratio [11], residual stress [12] and thermal conductivity [13] have been studied extensively. There are many existing approaches to determine the CTEs of thin films [14–17]. Out-of-plane deformations of test cantilevers caused by thermal expansion have been employed to measure the CTEs of thin films [14]. The out-of-plane deformation is measured precisely using a white light interferometer. The CTEs of silicon-based films have been directly determined by in-plane thermal expansion measured using an optical microscope [15, 16]. Due to the limited resolution of optical microscopes, a micro structure to magnify the in-plane thermal expansion is required. The well-known wafer curvature technique has been employed to monitor the average global CTE of thin films [17]. The techniques in [14, 17] are simple and can determine the CTE of an as-deposited single-layer thin film.

In short, the existing techniques determine the CTEs and elastic moduli of thin films using single-layer or bi-layer MEMS structures. However, the standard CMOS process consists of various metal and dielectric thin films. For instance, the Taiwan Semiconductor Manufacture Company (TSMC) 0.35 μm 2P4M CMOS process has four metal layers and four dielectric layers, as shown in figure 1(*a*). As a result, it is a challenge to determine the CTEs of the multilayer metal and dielectric films of CMOS processes (e.g. the eight metal and dielectric layers of the 2P4M CMOS process) using existing approaches. Thus, based on the CMOS process, this study designs and implements test cantilevers with stacking of different metal–dielectric layers. Furthermore, an auxiliary Si cantilever on a SOI wafer is also fabricated. With the proposed test cantilevers and the related testing methods in this study, the concept in [14] can be extended to determine the CTEs of metal and dielectric films for a standard CMOS process. In application, the TSMC 0.35 μm 2P4M CMOS process shown in figure 1(*a*) is employed as the study case. Such a 2P4M standard CMOS process consists of four metal layers (M1–M4) for electric routing, and four dielectric layers (including one inter-layer-dielectric (ILD) layer and three inter-metal-dielectric (IMD1–3) layers) for electric isolation. Based on the TSMC 2P4M CMOS process, the eight test cantilevers with different stacked layers have been designed and fabricated, as shown in figure 1(*b*). The static out-of-plane thermal deformation of the test cantilevers with temperature change is measured using an optical interferometer, and thus the CTEs of the metal and dielectric films are determined. Note that to extract the CTE using the proposed approach, the elastic modulus has to be determined in advance. This approach could be further exploited to determine the CTEs of thin films fabricated using other standard CMOS processes, for example the 1P6M process.

2. Fabrication processes for test cantilevers

Figure 1(*a*) displays the stacked layers for the standard TSMC 2P4M CMOS process. Based on the stacking of these layers, this study designs and implements the eight test cantilevers shown in figure 1(*b*). Such a test cantilever has a simple analytical model and can easily be fabricated. These eight cantilevers with different stacked layers can help to determine the CTEs and elastic moduli of the metal and dielectric films. As reported in [18], the dielectric layers of the standard CMOS process are categorized as ILD and IMD films. Thus, as indicated in figure 1(*b*), the stacked layers of the four metal–dielectric test cantilevers are, respectively, M1/ILD, M2/IMD1/ILD, M3/IMD12/ILD and M4/IMD123/ILD. Moreover, the stacked layers for the pure dielectric test cantilevers are, respectively, ILD, IMD1/ILD, IMD12/ILD and IMD123/ILD. IMD12 denotes a composite layer with stacking of IMD1 and IMD2 films (similarly, the IMD123 composite layer denotes the stacking of IMD1, IMD2 and IMD3 films).

Figure 2 shows the process flow to prepare the test cantilevers in figure 1(*b*) for the CTE extraction of CMOS layers. Figure 2(*a*) shows the stacked layers and patterning after the standard 2P4M CMOS processes by TSMC. After this, the post-CMOS processes in figures 2(*b*)–(*d*) were employed to implement the test cantilevers. As shown in figure 2(*b*), H_2SO_4 and H_2O_2 solutions were employed to etch the metal films and tungsten vias to define the planar dimensions of the test cantilevers. The metal films to form the test cantilevers were protected by the dielectric films during the metal wet etching. The dielectric films for the protection of metal layers were then removed by reactive ion etching (RIE). Thus, the width of the metal film was smaller than that of the dielectric layer. After this, the metal–dielectric test cantilevers were suspended by XeF_2 silicon isotropic etching, as shown in figure 2(*c*). Thus, the metal–dielectric test cantilevers shown in figure 1(*b*) were implemented. After the resonant frequency and the bending curvature versus temperature change of the test cantilevers in figure 2(*c*) were characterized, the top metal layers of these beams were removed by the H_2SO_4 and H_2O_2 solutions, as shown in figure 2(*d*). Thus, the pure dielectric (IMD/ILD) test cantilevers shown in figure 1(*b*) were also fabricated. The resonant frequency and the bending curvature versus temperature change of these dielectric layer test cantilevers were also characterized.

Meanwhile, the auxiliary Si test cantilevers were fabricated on the SOI wafer, as shown in figures 2(*e*) and (*f*). The typical beam length and thickness of the auxiliary Si test cantilever were 700 μm and 25 μm, respectively. As shown in figure 2(*e*), deep RIE (DRIE) was employed to define the planar dimensions of the auxiliary Si cantilever. The sacrificial oxide layers were removed using hydrofluoric acid solution to suspend the auxiliary Si beams, as shown in figure 2(*f*). Finally, the test cantilevers in figures 2(*d*) and

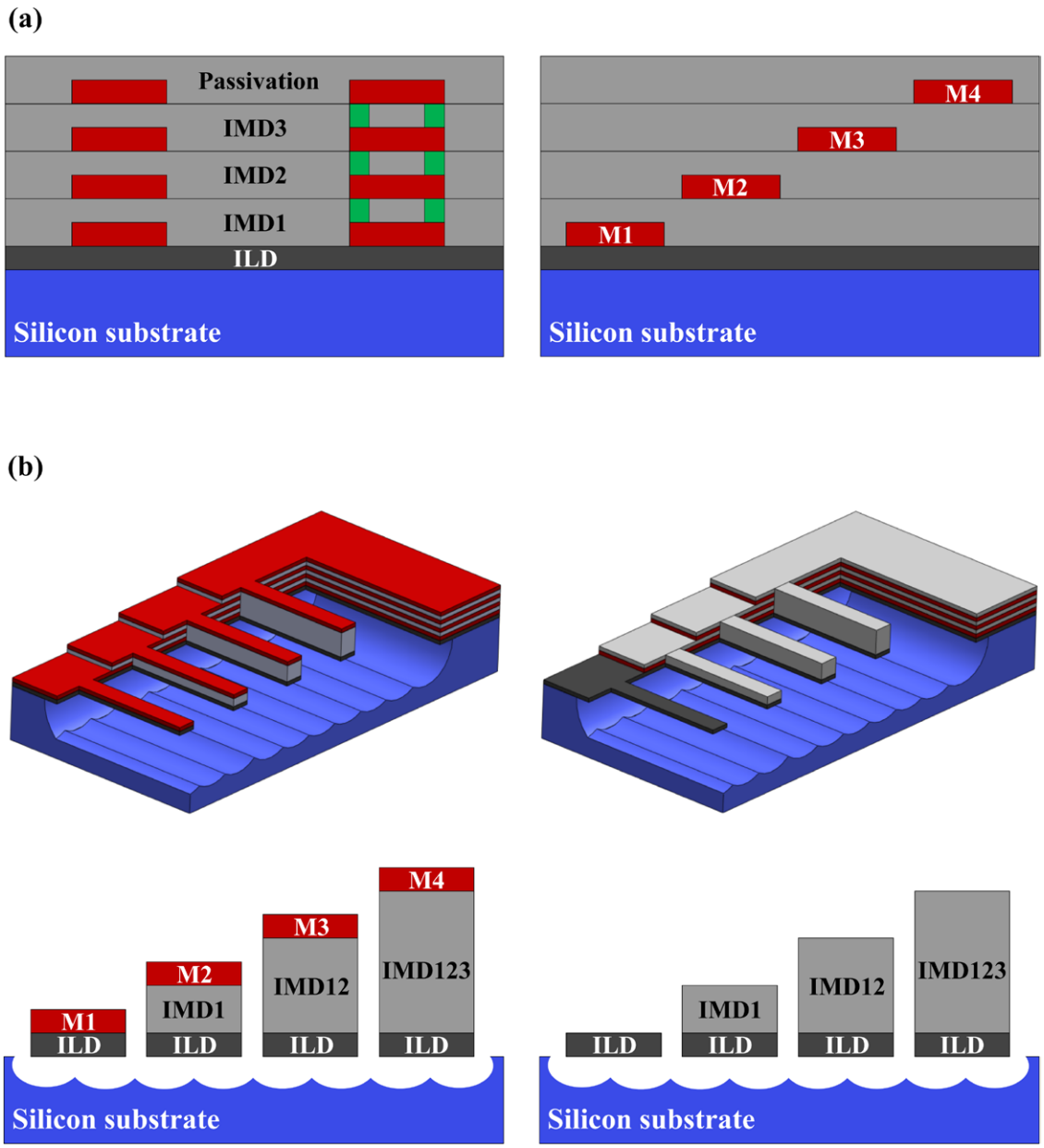

Figure 1. (*a*) The stacked layers for the standard TSMC 0.35 μm 2P4M process and (*b*) the eight test cantilevers consisting of different CMOS stacked layers.

(*f*) were simultaneously deposited with 0.5 μm assistant Al film by evaporation. Thus, the Al/ILD and Al/Si films of the bi-layer cantilevers were implemented, respectively, on the CMOS and SOI chips, as shown in figures 2(*g*) and (*h*). Since the material properties of the Si device layer were known in advance, the material properties of the assistant Al film could be extracted using the Al/Si bi-layer cantilever on the SOI chip in figure 2(*h*). Then, the material properties of the CMOS ILD layer could be extracted using the Al/ILD bi-layer cantilever on the CMOS chip in figure 2(*g*). When the material properties of the dielectric ILD film were obtained, the CTEs and elastic moduli of the four different metal films (M1–M4) and the dielectric layers underneath could be determined using the measured resonant frequencies and bending curvatures on the eight metal–dielectric and IMD/ILD test cantilevers in figures 2(*c*) and (*d*). Section 3 will discuss further the approach to determine the CTEs and elastic moduli of these films.

3. Concept and approach

This section describes the model and approach to determine the CTEs and elastic moduli of the metal and dielectric films using the eight metal–dielectric and IMD/ILD test cantilevers displayed in figure 1(*b*). Note that each of the metal layers (M1–M4) in figure 1(*a*) consist of AlCu and TiN. The composition of each metal and dielectric layer is reported in [19]. Moreover, the IMD12 (stacking of IMD1 and IMD2) and IMD123 (stacking of IMD1, IMD2 and IMD3) in figure 1(*b*) are also composite dielectric layers. To simplify the model, the equivalent mechanical and thermal properties for these

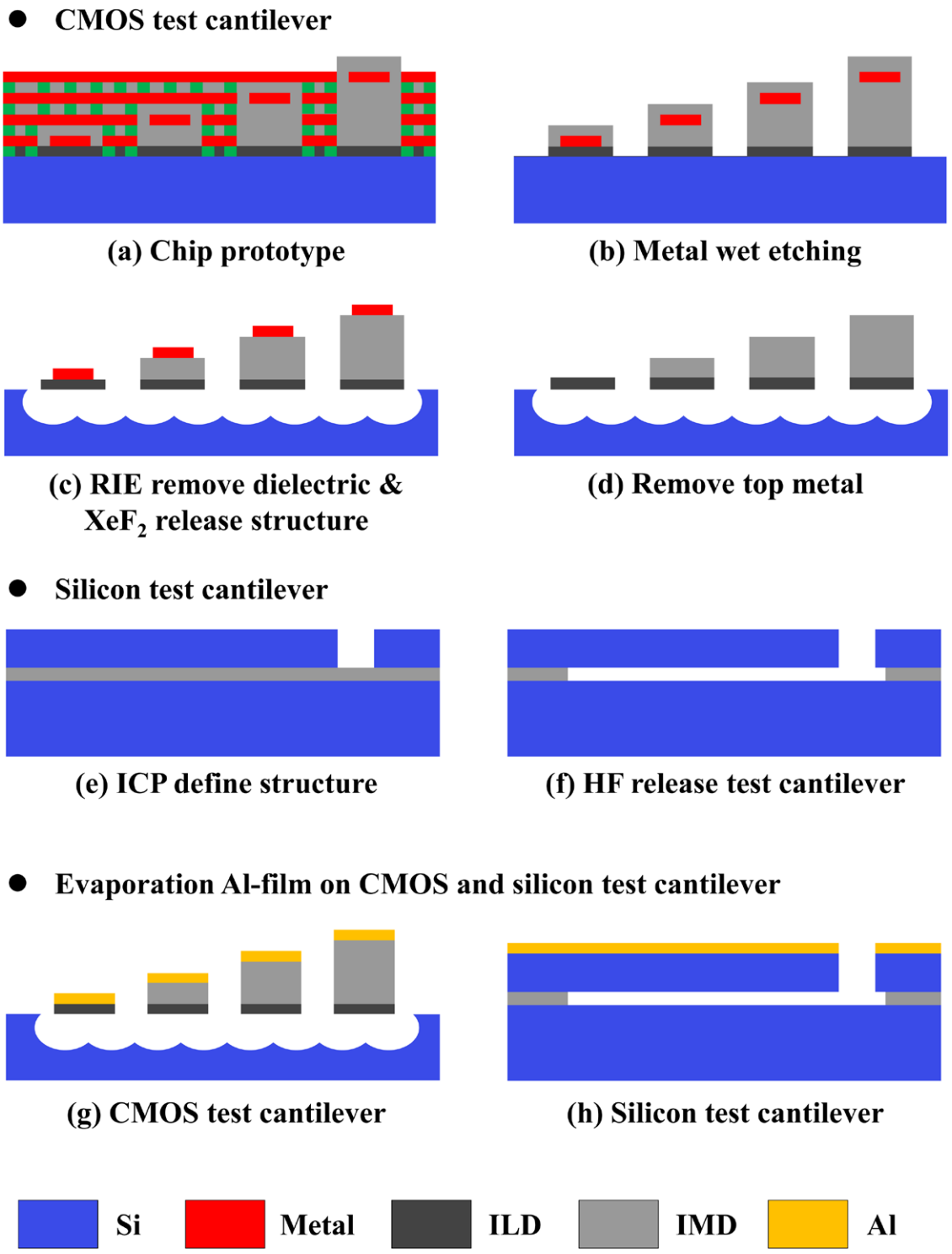

Figure 2. The process flows for the implementation of (*a*)–(*d*) test cantilevers consisting of CMOS layers, (*e*), (*f*) the Si test cantilevers and (*g*), (*h*) the assistant Al film simultaneously deposited on the CMOS and Si test cantilevers.

composite dielectric (IMD12 and IMD123) and metal (M1–M4) layers are considered in this study.

3.1. Analysis for test cantilevers

As indicated in figure 3(*a*), the bi-layer cantilever of length L consists of two thin films (Layer1 and Layer2) with elastic moduli of E_1 and E_2, CTEs of α_1 and α_2, thicknesses of h_1 and h_2 and widths of b_1 and b_2. According to the mismatch of CTEs between two films, the bi-layer cantilevers will be bent out-of-plane with a constant radius of curvature R when temperature changes [14]. The relationship between the radius of curvature R of the bi-layer cantilever and the temperature change ΔT can be expressed as [20–22]

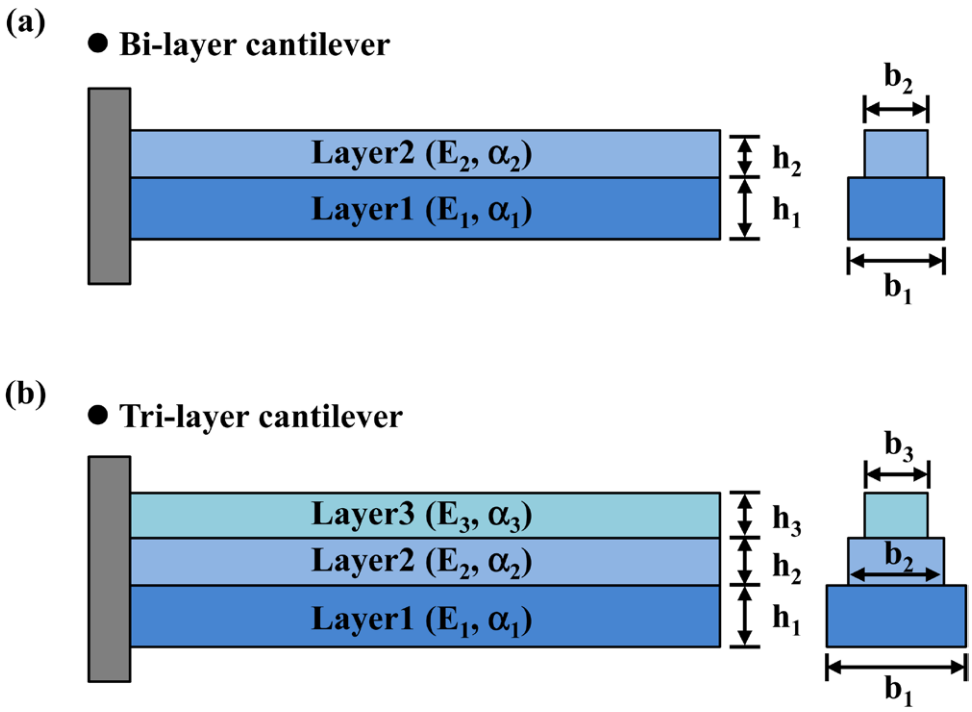

Figure 3. The (*a*) bi-layer cantilever and (*b*) tri-layer cantilever models to determine the elastic moduli and CTEs of the CMOS thin films.

$$\frac{1}{R} = \frac{6[s_1 s_2 h(\alpha_1 - \alpha_2)]\Delta T}{3(s_1 s_2)h^2 + (E_1 b_1 h_1^3 + E_2 b_2 h_2^3)(s_1 + s_2)} \tag{1}$$

where h is the total film thickness of the bi-layer cantilever ($h = h_1 + h_2$), and the parameters s_1 and s_2 are, respectively, expressed as $s_1 = E_1 h_1$ and $s_2 = E_2 h_2$. For the tri-layer cantilever shown in figure 3(*b*), the mismatch of CTEs between the thin films will also cause the bending of the beam during a temperature change. The relationship between the radius of curvature R of the tri-layer beam and the temperature change ΔT becomes [20–22]

$$\frac{1}{R} = \frac{\begin{array}{l}6[s_1 s_2(h_1 + h_2)(\alpha_1 - \alpha_2) + s_1 s_3(h_1 + 2h_2 + h_3)(\alpha_1 - \alpha_3) \\ + s_2 s_3(h_2 + h_3)(\alpha_2 - \alpha_3)]\Delta T\end{array}}{\begin{array}{l}3[s_1 s_2(h_1 + h_2)^2 + s_1 s_3(h_1 + 2h_2 + h_3)^2 \\ + s_2 s_3(h_2 + h_3)^2] + (E_1 b_1 h_1^3 + E_2 b_2 h_2^3 + E_3 b_3 h_3^3) \\ (s_1 + s_2 + s_3)\end{array}} \tag{2}$$

where E_3 is the elastic modulus, α_3 is the CTE, h_3 and b_3 are the thickness and width, and the parameters s_3 is expressed as $s_3 = E_3 h_3$ for Layer3. As indicated in (1) and (2), the temperature change ΔT is a controlled parameter. The radius of curvature R is measured using the optical interferometer. In addition, the film thickness h and width b are measured using existing approaches. Thus, the CTEs α_1, α_2 and α_3 can be extracted from (1) and (2) as the elastic moduli E_1, E_2 and E_3 are determined.

The elastic modulus E_1 of the film can be determined from the resonant frequencies of the single-layer cantilever formed by Layer1 [10]. From the Euler–Bernoulli beam model, the relationship between the elastic modulus E_1 and the resonant frequency of the first out-of-plane bending mode f_{single} for the single-layer cantilever can be expressed as [23]

$$E_1 = \frac{48\pi^2}{(1.87)^4}\frac{L^4}{h_1^2}\rho_1\left(f_{\text{single}}\right)^2 \tag{3}$$

where ρ_1 is the material density of Layer1, and L is the length of the cantilever. Thus, the elastic modulus E_1 of Layer1 can be determined from (3) as the resonant frequency of the single-layer cantilever is measure. After that, the elastic moduli of films E_2 and E_3 can be determined from the resonant frequencies of the bi-layer and tri-layer test cantilevers indicated in figure 3. The relationship between the elastic modulus E_2 and the resonant frequency of the first out-of-plane bending mode f_{bilayer} for the bi-layer cantilever (consisting of Layer1 and Layer2) can be expressed as [23–25]

$$E_2 = \frac{4\pi^2}{(1.87)^4}\frac{1}{C_{b2}}\left(\rho_1 b_1 h_1 + \rho_2 b_2 h_2\right)L^4\left(f_{\text{bilayer}}\right)^2 - \frac{C_{b1}}{C_{b2}}E_1 \tag{4}$$

where ρ_2 is the material density of Layer2 and the parameters C_{b1} and C_{b2} are respectively expressed as

$$C_{b1} = \left(\frac{b_1 h_1^3}{12}\right) + b_1 h_1\left[\frac{(h_1 + h_2)(b_2 h_2)}{2(c_1 b_1 h_1 + b_2 h_2)}\right]^2 \tag{5}$$

$$C_{b2} = \left(\frac{b_2 h_2^3}{12}\right) + b_2 h_2\left[\frac{(h_1 + h_2)(c_1 b_1 h_1)}{2(c_1 b_1 h_1 + b_2 h_2)}\right]^2 \tag{6}$$

where c_1 is the ratio of the thin film elastic moduli ($c_1 = E_1/E_2$). As the resonant frequency of the bi-layer cantilever is measured and the elastic modulus E_1 of Layer1 is extracted from (3), the elastic modulus E_2 of Layer2 can be further determined from (4)–(6). Moreover, the relationship between the

equivalent elastic modulus E_3 and the first resonant frequency of the out-of-plane bending mode f_{trilayer} of the tri-layer cantilever (consisting of Layer1, Layer2 and Layer3) can be expressed as [23–25]

$$E_3 = \frac{4\pi^2}{(1.87)^4}\frac{1}{C_{t3}}\left(\rho_1 b_1 h_1 + \rho_2 b_2 h_2 + \rho_3 b_3 h_3\right) L^4 \left(f_{\text{trilayer}}\right)^2 - \frac{C_{t1}}{C_{t3}}E_1 - \frac{C_{t2}}{C_{t3}}E_2 \tag{7}$$

where ρ_3 is the material density of Layer3 and the parameters C_{t1}, C_{t2} and C_{t3} are, respectively, expressed as

$$C_{t1} = \left(\frac{b_1 h_1^3}{12}\right) + b_1 h_1\left[\frac{(h_1+h_2)(c_2 b_2 h_2)+(h_1+2h_2+h_3)(b_3 h_3)}{2(c_3 b_1 h_1 + c_2 b_2 h_2 + b_3 h_3)}\right]^2 \tag{8}$$

$$C_{t2} = \left(\frac{b_2 h_2^3}{12}\right) + b_2 h_2\left[\frac{(h_1+h_2)(c_3 b_1 h_1 + b_3 h_3)-(h_1+2h_2+h_3)(b_3 h_3)}{2(c_3 b_1 h_1 + c_2 b_2 h_2 + b_3 h_3)}\right]^2 \tag{9}$$

$$C_{t3} = \left(\frac{b_3 h_3^3}{12}\right) + b_3 h_3\left[\frac{(h_1+2h_2+h_3)(c_3 b_1 h_1 + c_2 b_2 h_2)-(h_1+h_2)(c_2 b_2 h_2)}{2(c_3 b_1 h_1 + c_2 b_2 h_2 + b_3 h_3)}\right]^2 \tag{10}$$

where c_2 and c_3 are the ratios of the thin film elastic moduli ($c_2 = E_2/E_3$ and $c_3 = E_1/E_3$). As the elastic moduli E_1 of Layer1 and E_2 of Layer2 are determined from (3)–(6), the elastic modulus E_3 of Layer3 can be extracted from (7)–(10) after the resonant frequency f_{trilayer} of the tri-layer cantilever is measured.

3.2. The CTE extraction approach using test cantilevers

By using the fabrication processes in figures 2(*a*)–(*d*), this study implements eight test cantilevers with different stacked layers of the TSMC 2P4M CMOS process. In addition, the auxiliary Al/Si and Al/ILD test cantilevers shown in figures 2(*g*) and (*h*) are also prepared on the SOI wafer and CMOS chip, respectively. Thus the elastic moduli and CTEs of the CMOS layers can be determined using the following steps.

***Step* 1.** First, the elastic modulus E_{ILD} of the ILD film is extracted from (3) using the ILD single-layer test cantilever in figure 2(*d*).

***Step* 2.** The CTE of the ILD film is further extracted using the auxiliary Al/Si and Al/ILD bi-layer cantilevers in figures 2(*g*) and (*h*). Since the CTE α_{Si} and elastic modulus E_{Si} of the single crystal Si cantilever are know in advance, the CTE α_{Al} and elastic modulus E_{Al} of the assistant Al film can be extracted from (1) and (4)–(6) using the Al/Si bi-layer cantilever in figure 2(*h*). The Si and ILD cantilevers are simultaneously deposited with the assistant Al film using the same process. Thus, the Al film on the Si cantilever has identical material properties (α_{Al} and E_{Al}) to that on the ILD cantilever. As α_{Al} and E_{Al} of the assistant Al film on top of the ILD cantilever and the elastic modulus E_{ILD} are known, the CTE α_{ILD} of the CMOS ILD film can also be extracted from (1) using the Al/ILD bi-layer cantilever in figure 2(*g*).

***Step* 3.** The CTE α_{IMD1} and elastic modulus E_{IMD1} of the CMOS IMD1 film are then extracted from (1) and (4)–(6) using the IMD1/ILD bi-layer cantilever shown in figure 2(*d*).

***Step* 4.** Following the same approach, the IMD12/ILD and IMD123/ILD bi-layer cantilevers in figure 2(*d*) can also be employed to extract, respectively, the equivalent elastic moduli E_{IMD12} and E_{IMD123} (and the equivalent CTEs α_{IMD12} and α_{IMD123}) of the IMD12 and IMD123 composite films.

***Step* 5.** As α_{ILD} and E_{ILD} of the ILD layer, and α_{IMD1} and E_{IMD1} of the IMD1 layer are known, the CTE α_{IMD2} and elastic modulus E_{IMD2} of the CMOS IMD2 film can be extracted from (2) and (7)–(10) using the tri-layer IMD2/IMD1/ILD cantilever shown in figure 2(*d*).

***Step* 6.** Similarly, the IMD3/IMD12/ILD tri-layer cantilever in figure 2(*d*) can be employed to extract the elastic modulus E_{IMD3} and the CTE α_{IMD3} of the CMOS IMD3 film.

***Step* 7.** After the material properties of the dielectric layers are determined, the equivalent elastic moduli and the CTEs of the composite metal films (AlCu and TiN) can be measured using the test cantilevers shown in figure 2(*c*). As α_{ILD} and E_{ILD} of the ILD layer are known, the equivalent CTE α_{M1} and elastic modulus E_{M1} of the M1 metal layer can also be extracted from, respectively, (1) and (4)–(6) using the M1/ILD bi-layer test cantilever shown in figure 2(*c*).

***Step* 8.** As α_{ILD} and E_{ILD} of the ILD layer, and α_{IMD1} and E_{IMD1} of the IMD1 layer are known, the equivalent CTE α_{M2} and elastic modulus E_{M2} of the M2 metal layer can be extracted from (2) and (7)–(10) using the tri-layer M2/IMD1/ILD test cantilever shown in figure 2(*c*).

***Step* 9.** Following the same approach, the M3/IMD12/ILD and M4/IMD123/ILD tri-layer cantilevers in figure 2(*c*) can also be employed to extract, respectively, the equivalent elastic moduli E_{M3} and E_{M4} (and the equivalent CTEs α_{M3} and α_{M4}) of the composite metal films.

4. Experiment and verification results

The scanning electron microscopy micrographs in figure 4 show the fabrication results of different types of CMOS MEMS cantilever beams. Figure 4(*a*) shows a cantilever array with different stacking of metal and dielectric layers after release. Figure 4(*b*) shows four cantilever arrays (marked by I, II, III and IV) with different stacking of metal and dielectric films. Each array has cantilevers of four different beam lengths and

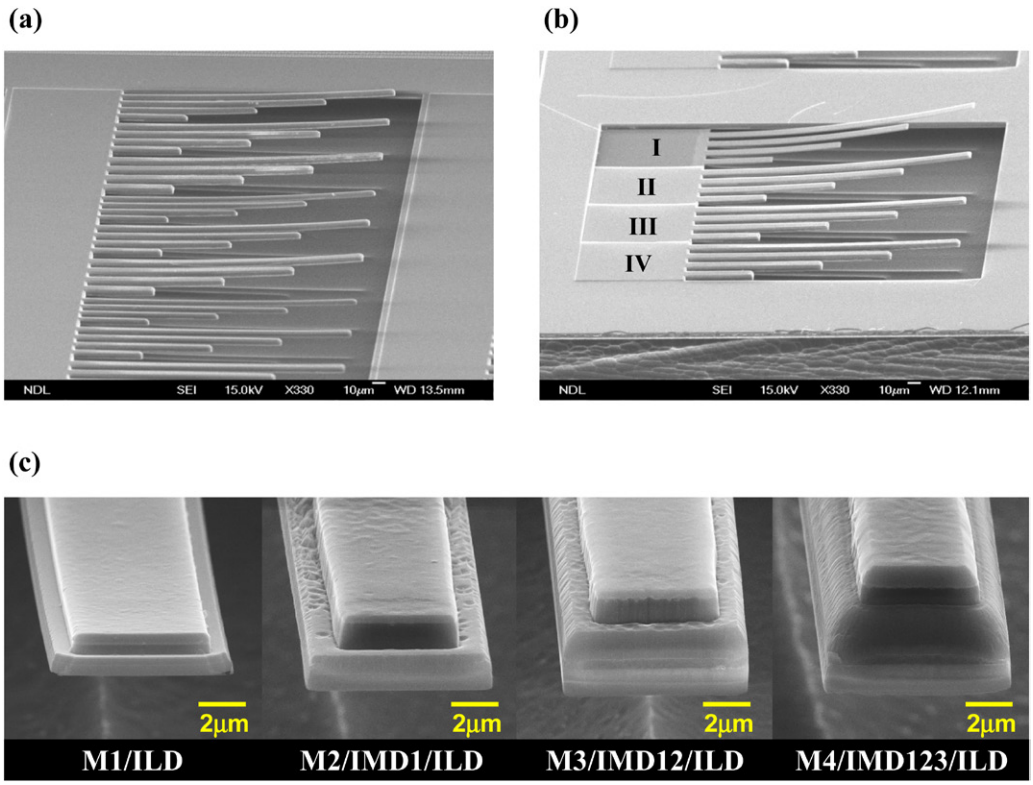

Figure 4. Typical fabrication results for (*a*) a cantilever array with different stacking of metal and dielectric layers after release and (*b*) four cantilever arrays marked by I, II, III and IV. The stacked layers of these four arrays are associated with those shown in figure 2(*c*). For example, the stacked layers of the cantilevers in arrays I and II are respectively M1/ILD and M2/IMD1/ILD. Each array has cantilevers of four different beam lengths. (*c*) The cross-section views of the test cantilevers in arrays I–IV.

the four cantilevers in each array (e.g. array I) have the same stacked layers. According to the residual stress of thin films, the test cantilevers have initial out-of-plane bending deformation after fabrication. The cantilevers in each beam array have the same stacked layers, and thus they have the same bending curvatures. Moreover, the cantilevers in different arrays (e.g. arrays I and II) have different bending curvature. The zoom-in micrograph in figure 4(*c*) shows the stacking of metal and dielectric layers for the test cantilevers displayed in figure 2(*c*). The test cantilevers designed in this study have a beam length ranging from 50–200 μm (50, 100, 150 and 200 μm) and a beam width of 8 μm, as displayed in figures 4(*a*) and (*b*). The experiments are mainly performed using the 200 μm long cantilever. As explained in the process steps, the width of the metal film is smaller than that of the dielectric film. Thus, the dimensions of the metal film on the test cantilever are reduced to 199.2 μm in length and 6.4 μm in width. This study measured the step heights of the unsuspended structures with eight different stacked layers, shown in figure 1(*b*) using a commercial optical interferometer (Veeco Inc., NT-1100). Therefore, the film thicknesses of each metal and dielectric layer were determined. This study further employed the concepts described in section 3.2 to measure the elastic moduli and CTEs of metal and dielectric films for the 2P4M CMOS process. Moreover, the uncertainties in the determination of the elastic moduli and CTEs for test cantilevers are based on the ISO guidelines in [26]. The confidence level of 95% is selected in this study to determine the expanded uncertainty value of measurement. A detailed explanation of the expanded uncertainty of measurement is given in the appendix.

4.1. Elastic modulus determination

As discussed in section 3, the equivalent elastic moduli of the metal and dielectric layers are determined using the resonant beam approach [10, 23–25]. In experiments, the post-CMOS fabrication processes will cause variations of dimensions and boundary conditions for the test cantilevers. As shown in figure 5, the boundary conditions of the test cantilever are changed due to the substrate undercut by XeF_2 silicon isotropic etching. Experiments indicate that an 8 μm undercut occurred at the boundary. According to finite element method (FEM) simulations, the boundary undercut will lead to a 2–3% decrease of natural frequency for 200 μm long test cantilevers. Thus, the decrease of measured natural frequencies predicted from FEM has been taken into account while extracting the elastic moduli of metal and dielectric layers from (3)–(10).

Figure 6(*a*) shows the measurement setup to characterize the dynamic response of the test cantilevers. The specimen is excited by a piezoelectric shaker and the dynamic response of the cantilever beam is measured using a commercial laser Doppler vibrometer (Polytec Inc., OFV 3001). Typical measured frequency responses in figure 6(*b*) show the resonant frequencies of eight test cantilevers (200 μm long) with

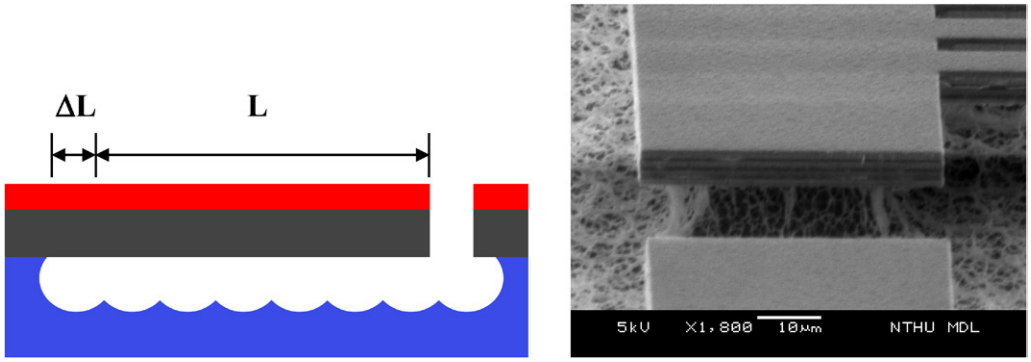

Figure 5. The boundary undercut of the test cantilever resulting from the post-CMOS process.

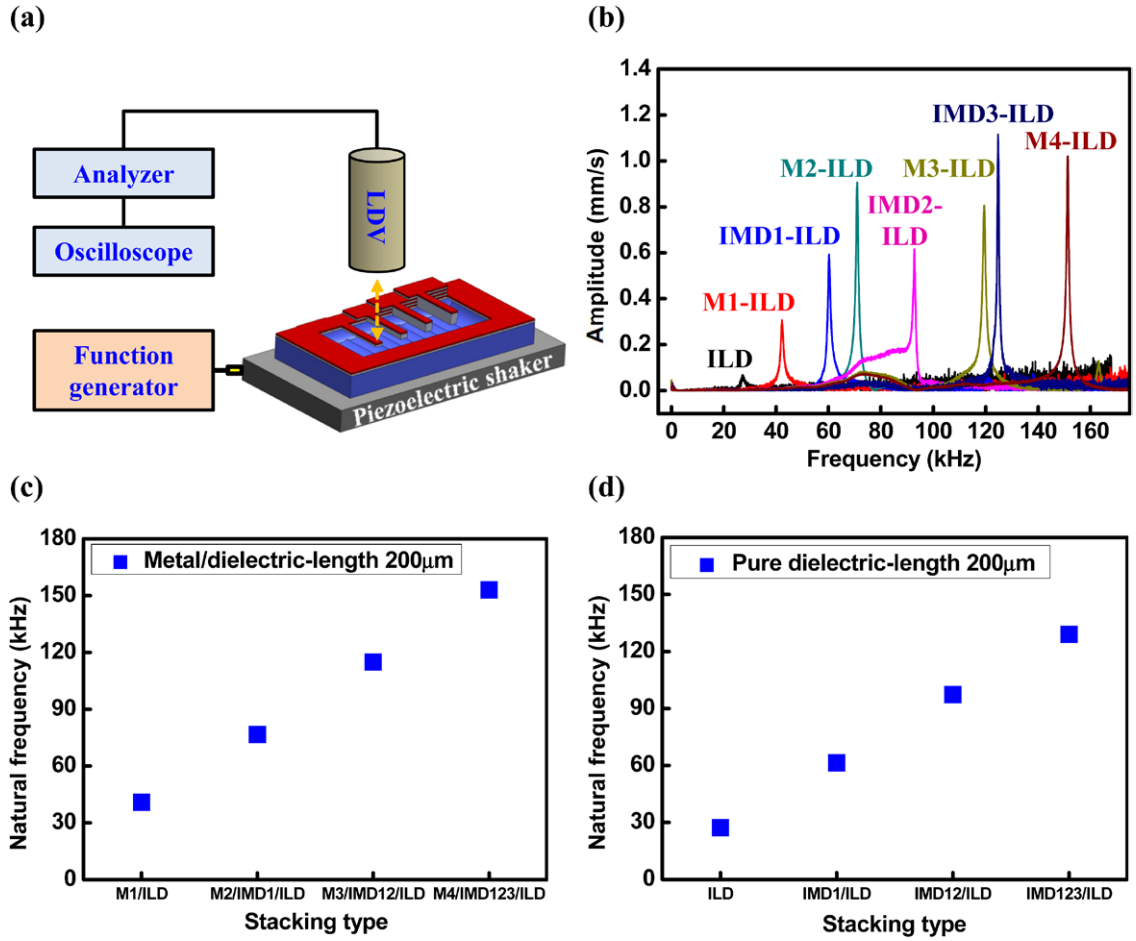

Figure 6. (*a*) The experimental setup to measure the natural frequency of the test cantilevers, (*b*) the typical measured natural frequencies of the first bending mode for the cantilevers with different stacked layers, (*c*) the natural frequencies of the 200 μm long cantilevers with stacked layers shown in figures 2(*c*) and (*d*) the natural frequencies of the 200 μm long cantilevers with stacked layers shown in figure 2(*d*).

different stacked layers (as indicated in figures 2(*c*) and (*d*). Figure 6(*c*) shows the natural frequencies measured from the 200 μm long metal–dielectric test cantilevers shown in figure 2(*c*). Figure 6(*d*) further shows the natural frequencies of the 200 μm long pure dielectric layer cantilevers in figure 2(*d*). The results are averaged from ten measurements on different test chips. From the measured film thickness, beam length and natural frequency of the single-layer ILD cantilever, the elastic modulus E_{ILD} of the CMOS ILD film was extracted from (3) (the natural frequency shift caused by boundary undercut has been taking into account). By following the steps in section 3.2, the elastic moduli of the other CMOS metal and dielectric films were determined from (4)–(10). In conclusion, the equivalent elastic moduli of four composite metal layers, M1–M4, were respectively 134.1 ± 6.0 GPa, 131.5 ± 10.8 GPa, 136.8 ± 16.9 GPa and 113.2 ± 14.8 GPa. Note that the expanded uncertainty values (6.0, 10.8, 16.9 and 14.8 GPa) for the elastic moduli of the metal layers are

Table 1. The elastic moduli and CTEs determined from the approach presented.

CMOS films	Elastic modulus	Expanded uncertainty	CTE	Expanded uncertainty
M4	113.2	14.8	18.1	1.6
M3	136.8	16.9	16.5	1.9
M2	131.5	10.8	16.9	2.0
M1	134.1	6.0	17.7	1.5
IMD123[a]	71.9	5.5	2.6	0.6
IMD12[b]	73.4	4.8	2.7	0.6
IMD3	74.8	7.6	2.6	0.5
IMD2	73.4	5.2	2.7	0.5
IMD1	73.8	2.7	2.6	0.7
ILD	76.9	1.3	2.7	0.7
Unit		GPa		10^{-6}/°C

[a] IMD123 denotes the stacking of IMD12 and IMD3 films.
[b] IMD12 denotes the stacking of IMD1 and IMD2 films.

determined from the approach in the appendix. The elastic moduli of dielectric layers ILD, IMD1, IMD2 and IMD3 were, respectively, 76.9 ± 1.3 GPa, 73.8 ± 2.7 GPa, 73.4 ± 5.2 GPa and 74.8 ± 7.6 GPa. Moreover, the equivalent elastic moduli of the composite dielectric layers IMD12 and IMD123 were, respectively, 73.4 ± 4.8 GPa and 71.9 ± 5.5 GPa. Table 1 summarizes the extraction results and their expanded uncertainty values. Due to the presence of TiN in the metal composite, the elastic moduli of the M1–M4 layers are much higher than those of the AlCu film. Moreover, the M4 film has a smaller equivalent elastic modulus since its TiN content is lower than the other metal layers.

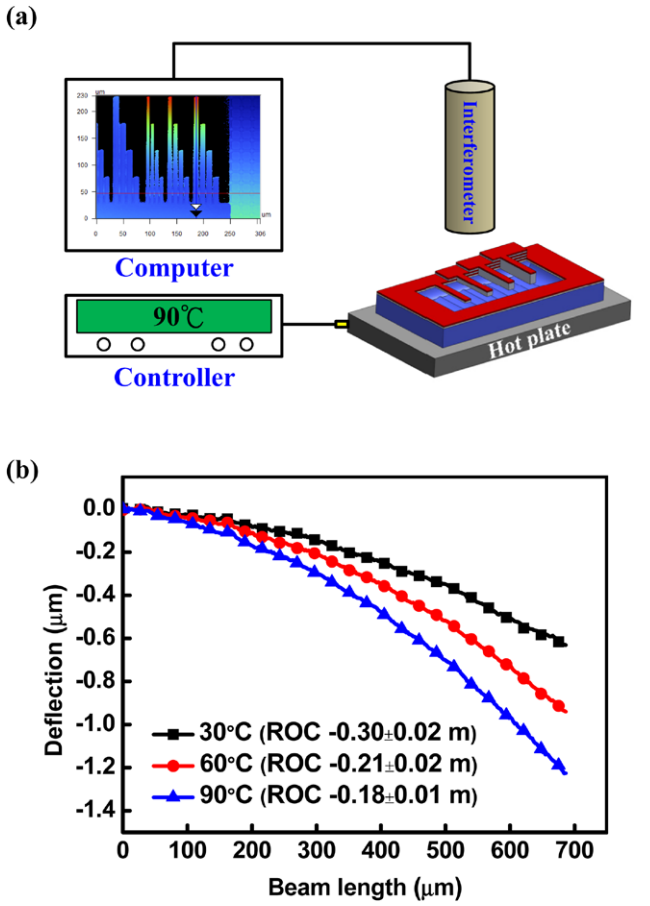

Figure 7. (*a*) The experimental setup to measure the static deformation of the cantilevers at different environment temperatures and (*b*) the typical measured deflection profiles of the Al/Si bi-layer cantilever at three different temperatures.

4.2. Determination of the coefficient of thermal expansion

After extracting the equivalent elastic moduli of the metal and dielectric layers, the CTEs of the CMOS thin films were extracted from (1)–(2) using the bending of the test cantilevers at given temperature elevations. According to the FEM simulations, the boundary undercut shown in figure 5 did not influence the bending curvature of the bi-layer test cantilevers. Thus, the boundary undercut effect was ignored while determining the CTE. The static thermal deformation of the test cantilevers was induced and measured using the experimental setup shown in figure 7(*a*). The test chip was heated by a heating stage with the temperature specified by the controller. Thermal deformation of the test cantilever was characterized using a commercial optical interferometer. The test chip was placed on the hot plate long enough to reach the thermal equivalent before measurement. The results in figure 7(*b*) show the deflection profiles of a 700 μm long auxiliary Al/Si bi-layer cantilever (consisting of a 0.5 μm thick Al film and a 25 μm thick silicon) measured at three different temperatures. Note that the heating temperatures on the hot plate were specified at 30, 60 and 90 °C by the controller. However, due to thermal resistance, the heating temperature on the test structure was dropped. In this study, the temperature distribution on the test chip was measured using an IR camera (FLIR, SC5000). The measurements in figure 8 characterize the surface temperature within 30–90 °C. The results indicate that the temperatures on the test chip surface were, respectively, 28.8 °C, 59.3 °C and 88.4 °C for the temperatures 30 °C, 60 °C and 90 °C. Thus, the drop of the heating temperature on the test cantilever is taken into account in the following measurements. Al film has a larger CTE than silicon and thus the tip deflection of the auxiliary Al/Si bi-layer beam was bent downward while the test chip was heated. The radius of curvature of the Al/Si cantilever changed from −0.30 ± 0.02 to −0.18 ± 0.01 m as the temperature changed from 30 to 90 °C. Since the CTE of single crystal silicon is 2.3 × 10^{-6} °C^{-1} [27], the CTE of the assistant Al film determined from (1) is (23.1 ± 1.8) × 10^{-6} °C^{-1} within the temperature range of 30–90 °C. In comparison with the existing results, the CTE of the Al film is 20.3 × 10^{-6} °C^{-1} in [14] and 25.0 × 10^{-6} °C^{-1} in [27]. The measurements in table 2 summarize the curvature variation of the bi-layer cantilevers (Al/ILD, IMD1/ILD, IMD12/ILD, IMD123/ILD and M1/ILD) and tri-layer cantilevers (IMD2/IMD1/ILD, IMD3/IMD12/ILD, M2/IMD1/ILD, M3/IMD12/ILD and M4/IMD123/ILD) as temperature changed from 30 to 90 °C. The radius of curvature of the Al/ILD cantilever changed from −2.28 ± 0.35 to −0.81 ± 0.09 mm as temperature

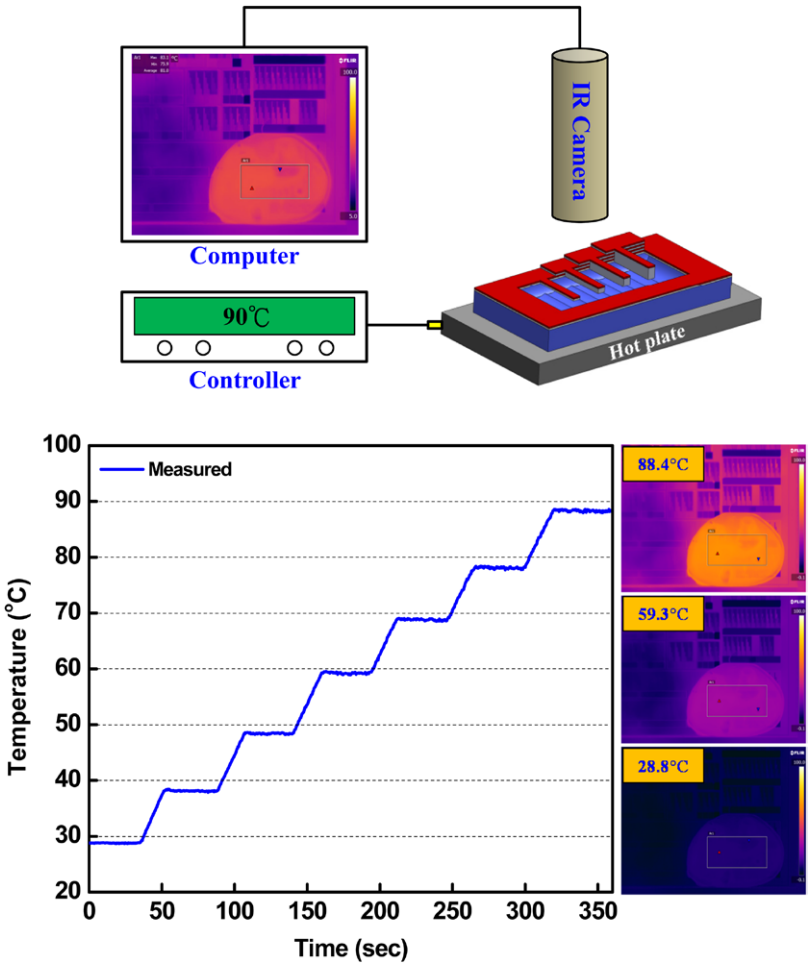

Figure 8. A comparison of the temperature variation of the test chip and hotplate using an IR camera.

changed from 30 to 90 °C. Since the CTE of the Al film is 23.1 × 10^{-6} °C^{-1}, the CTE of the CMOS ILD film determined from (1) is (2.7 ± 0.7) × 10^{-6} °C^{-1} within the temperature range of 30–90 °C. Similarly, according to the measured curvature change of the bi-layer cantilevers in table 2, the CTEs of the IMD1, IMD12, IMD123 and M1 layers extracted from (1) are, respectively, (2.6 ± 0.7) × 10^{-6} °C^{-1}, (2.7 ± 0.6) × 10^{-6} °C^{-1}, (2.6 ± 0.6) × 10^{-6} °C^{-1} and (17.7 ± 1.5) × 10^{-6} °C^{-1}. Then, using the curvature change of the IMD2/IMD1/ILD and IMD3/IMD12/ILD tri-layer cantilevers, the CTEs of the IMD2 and IMD3 layers extracted from (2) are, respectively, (2.7 ± 0.5) × 10^{-6} °C^{-1} and (2.6 ± 0.5) × 10^{-6} °C^{-1}. Finally, the CTEs of the metal films M2, M3, and M4 extracted, respectively, from the tri-layer cantilevers M2/IMD1/ILD, M3/IMD12/ILD, and M4/IMD123/ILD are, respectively, (16.9 ± 2.0) × 10^{-6} °C^{-1}, (16.5 ± 1.9) × 10^{-6} °C^{-1} and (18.1 ± 1.6) × 10^{-6} °C^{-1}. Table 1 summarizes the measured CTEs of the metal and dielectric films.

Table 2. The measured radius of curvature for the bi-layer and tri-layer cantilevers with various stacked layers at two different environment temperatures.

CMOS films	Radius of curvature (30 °C)	Radius of curvature (90 °C)
M4/IMD123/ILD	2.09 ± 0.26	3.07 ± 0.58
M3/IMD12/ILD	1.89 ± 0.23	2.73 ± 0.52
M2/IMD1/ILD	0.97 ± 0.03	1.30 ± 0.06
M1/ILD	0.22 ± 0.02	0.26 ± 0.03
IMD123/ILD	4.13 ± 0.47	4.11 ± 0.48
IMD12/ILD	2.95 ± 0.40	2.94 ± 0.38
IMD1/ILD	1.07 ± 0.02	1.07 ± 0.02
Al/ILD	−2.28 ± 0.35	−0.81 ± 0.09
Unit	mm	mm

4.3. Verification results

In addition to the test cantilevers in figure 1(*b*), this study has also designed and implemented cantilevers with different stacked layers as shown in figure 9(*a*) to confirm the accuracy of the extracted elastic moduli and CTEs. Note that the cantilevers #8, #12, #14 and #15 in figure 9(*a*) and the metal–dielectric test cantilevers in figure 1(*b*) have the same stacked layers. This study establishes the FEM models for the cantilevers shown in figure 9(*a*), and the elastic moduli and CTEs extracted from this study (as listed in table 1) are

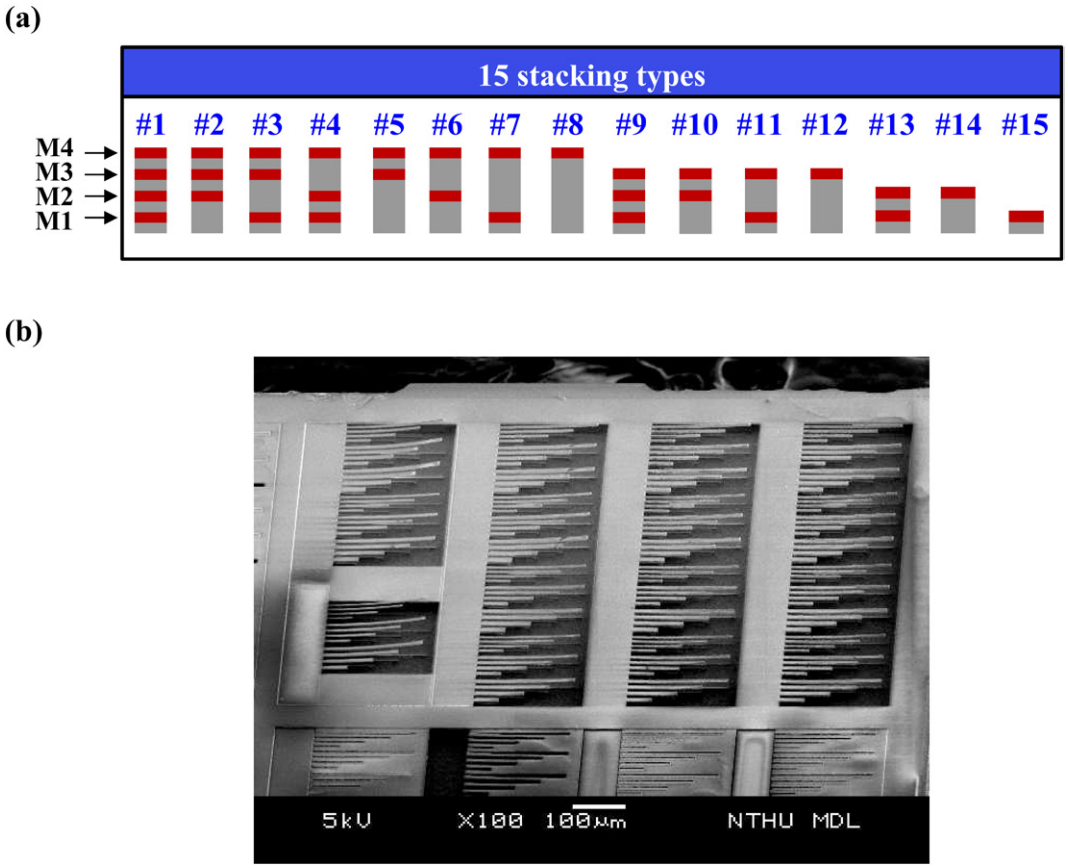

Figure 9. The cantilevers of fifteen different stacked layers are (*a*) designed and (*b*) implemented to confirm the measured elastic moduli and CTEs of the CMOS films.

used in the model. Thus, the resonant frequencies and out-of-plane thermal deformations of these 15 cantilevers can be predicted from the FEM simulations. To verify the results predicted from the FEM simulations, these multilayer cantilevers have also been fabricated using the post-CMOS processes in figures 2(*a*)–(*d*). Figure 9(*b*) shows the typical fabricated cantilevers used for the measurements.

Figure 10(*a*) shows the measured and predicted results for the natural frequencies of these 15 cantilevers. The cantilevers used for the measurements and simulation are 200 μm long and 8 μm wide. Note that the variations of beam dimensions and boundary conditions caused by the fabrication processes have been taken into account in the FEM simulation model. The deviations between the simulation predictions and the measurements for these 15 cantilevers are less than 5%. Thus, the simulation results agree well with the measurements which indicate that the current approach can precisely determine the elastic moduli of CMOS films. Moreover, figure 10(*b*) shows the measured and predicted results for the out-of-plane tip deflections of the 15 cantilevers at a 60 °C temperature elevation. Note that the initial deflection (at room temperature) of the cantilevers caused by the thin film residual stresses has been taken into account and specified in the FEM model. As a result, the simulation predictions and the measurements for these 15 cantilevers have deviations ranging between 0.2–15.9%. Similarly, the simulation results agree well with the measurements and thus the approach presented here can determine reasonably well the CTEs of CMOS films.

4.4. Discussion

An approach to determine the elastic moduli and CTEs of CMOS thin films using micro-machined bi-layer and tri-layer cantilevers has been presented in this study. The test cantilevers were implemented using the post-CMOS fabrication process shown in figures 2(*c*) and (*d*). The film thickness is also a critical parameter when extracting the elastic moduli and CTEs using this approach. Thus, the thickness of each CMOS metal and dielectric layer has been measured to prevent its variation after the post-CMOS process. In addition, when preparing the auxiliary Al/Si and Al/ILD test cantilevers on the SOI wafer and CMOS chip (as shown in figures 2(*g*) and (*h*)), the thickness uniformity of the Al film is of importance. In this study, the Al film was simultaneously deposited on the CMOS and SOI chips. Moreover, the deposition of the Al film on the ILD and Si cantilevers was a die level process. The test chip (2 mm × 2 mm) with the ILD cantilever and the test chip (3 mm × 3 mm) with the Si cantilever were placed side by side on a carry wafer during the Al film deposition. Thus, the thickness variation of the Al film in the Al/ILD and Al/Si test structures was ignored.

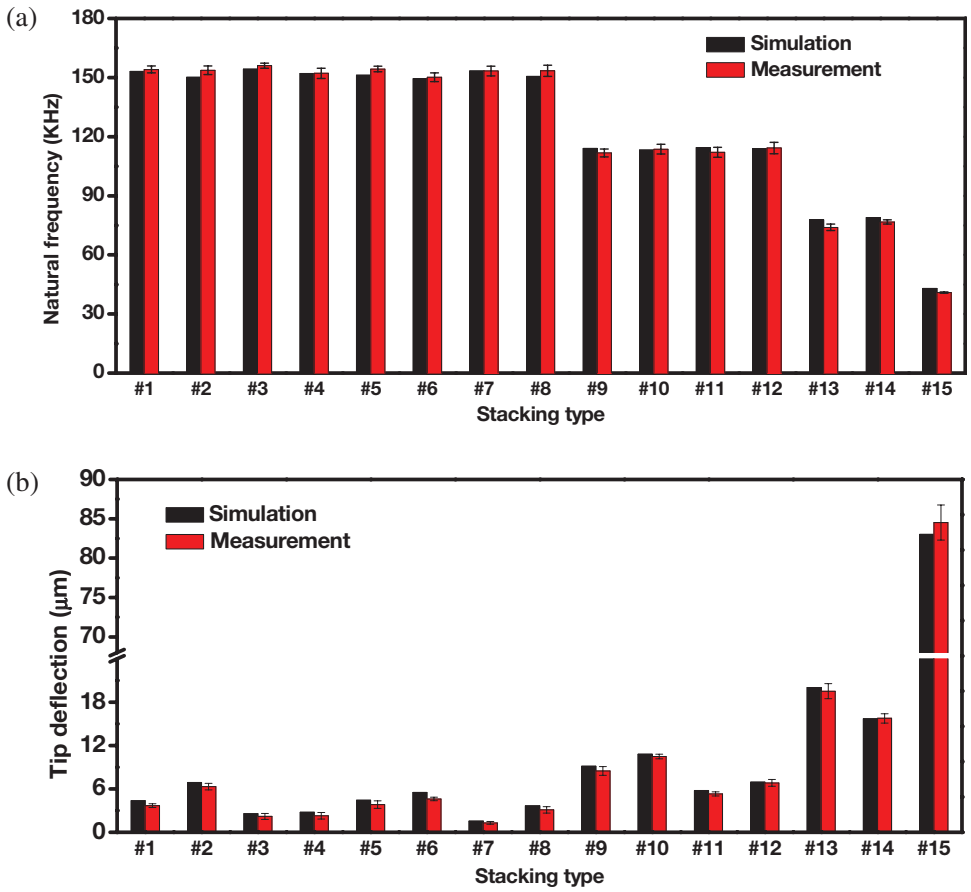

Figure 10. A comparison of the simulation and measurements of (*a*) the natural frequency and (*b*) the thermal deformation at a 60 °C temperature elevation of the 15 test cantilevers in figure 9.

The uncertainty analysis results for the 95% confidence level have been listed in table 1. The process uniformity and reproducibility from ten chips have been taken into account in the expanded uncertainty. Moreover, the imperfect geometry and boundary of the test cantilevers fabricated by the post-CMOS process will affect the nominal values in table 1. Hence, the analytical and simulation models need to be modified to consider the various effects introduced by the fabrication processes. For instance, the XeF_2 isotropic etch will cause the problem of boundary undercut for the test cantilevers. Therefore, as discussed in section 4.1, the natural frequency of the cantilevers is decreased due to boundary undercut, which further influences the determined elastic moduli. However, as discussed in section 4.2, the bending curvature of the bi-layer cantilever will not be influenced by the boundary undercut. Thus, the boundary undercut is ignored in the bi-layer cantilever model for CTE extraction.

Moreover, the dielectric layer removed by RIE for the fabrication shown in figure 2(*c*) is a time control process. Since the metal film did not cover the whole dielectric layer underneath, over-etching of the dielectric layer may also occur. In this study, the dielectric layer etching time was determined using test samples. After that, the cantilevers were fabricated based on this process recipe. However, to ensure the full exposure of metal layer edges for all samples, the etching time was slightly longer than the recipe. Thus, some of the dielectric layers below the metal film were over-etched by nearly 0.1–0.2μm. As a result, the over-etching of the dielectric layer causes a natural frequency variation of 0.4–1.0%, and leads to a 1.7–4.4% error to the extracted elastic moduli. Moreover, the bending curvature has a variation of 0.8–1.6% and leads to a 1.5–2.8% error to the CTEs. Note that the non-perfect rectangular cross-section caused by RIE, as shown in figure 4(*c*), is ignored in this study.

5. Conclusions

In summary, this study presented an approach to determine the CTEs of metal and dielectric films for a standard CMOS process using bi-layer and tri-layer test cantilevers. Cantilevers of different stacked metal–dielectric layers have been designed and implemented for measurements. Moreover, auxiliary Si test cantilevers and an assistant Al film are critical to realize the Al/ILD and Al/Si bi-layer cantilevers on CMOS and SOI chips. The CTE of the ILD film is thus determined. Note that the imperfect boundary conditions and the deviations of the beam dimensions resulting from the process have to be taken into account in the model. Measurements indicate that the CTEs of the M1–M4 layers ranged from $(16.5 \pm 1.9) \times 10^{-6}\,°C^{-1}$ to $(18.1 \pm 1.6) \times 10^{-6}\,°C^{-1}$. Moreover, the determined CTEs of the CMOS dielectric layers ILD and IMD1–3 ranged from $(2.6 \pm 0.5) \times 10^{-6}\,°C^{-1}$ to $(2.7 \pm 0.7) \times 10^{-6}\,°C^{-1}$. Table 1

summarizes the measured CTEs and elastic moduli of the metal and dielectric films for standard 2P4M CMOS processes. This study has also designed and implemented 11 additional cantilevers with different stacked layers to confirm the elastic moduli and CTEs extracted from the approach presented. By using the CTEs and elastic moduli measured in this study, the natural frequencies and thermal deformations of these cantilevers were predicted from the simulation model. The simulation results agree well with the measurements. Thus, the CTEs and elastic moduli of the CMOS films determined from the approach presented here could be employed to predict the mechanical characteristics of CMOS MEMS devices implemented using the TSMC 0.35 μm 2P4M CMOS process. The presented method can be further extended to determine the CTEs and elastic moduli of metal and dielectric films for other CMOS processes.

Acknowledgments

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Appendix

As reported in [26], the variable y to be determined in this study (such as the CTE) has the combined standard uncertainty $u_c(y)$,

$$u_c(y)=\left[\sum_{i=1}^{n}\left(\frac{\partial y}{\partial x_i}\right)^2 u^2(x_i)\right]^{\frac{1}{2}} \quad \text{(A.1)}$$

where x_i ($i = 1 \sim n$) are the measurement variables (such as the film thickness, the length and width of the test cantilevers, the natural frequency of the test cantilevers, heating temperature, etc), $(\partial y/\partial x_i)$ ($i = 1 \sim n$) are the sensitivity coefficients and $u(x_i)$ ($i = 1 \sim n$) are, respectively, the standard uncertainties of these variables. In this study, the uncertainty introduced from the measurement and fabrication processes is considered. The standard uncertainty for the determined thin film CTEs is evaluated based on (1) and (2). Moreover, the standard uncertainty for the determined thin film elastic moduli is estimated based on (3)–(10). Note that the out-of-plane dimension of the test cantilever measured using a commercial optical interferometer has a resolution of 3 nm and the in-plane dimensions of the test cantilevers measured using a commercial optical microscope (Olympus, STM6) are 0.1 μm. The standard uncertainty of the radius of curvature measured using a commercial optical interferometer is estimated as 0.3% from a series measurement for system repeatability [26]. The natural frequency measured using a commercial laser Doppler vibrometer has a resolution of 10 Hz. Moreover, the heating temperature specified using a commercial hot plate (Linkam Ltd, THMS600) has a resolution of 0.1 °C. Furthermore, the process uniformity may lead to the variation of measurements. The reproducibility of the measurement results for ten different chips is also considered in the standard uncertainty. The standard uncertainties of measurement variables $u(x_i)$ in (A.1) are determined accordingly. After that, the combined standard uncertainties $u_c(y)$ of the elastic modulus and CTE for each CMOS layer are determined based on (A.1). The expanded uncertainty is further expressed as [26]

$$U = ku_c(y) \quad \text{(A.2)}$$

where k is the coverage factor. The confidence level is selected as 95% in this study and thus the coverage factor is approximately 2. The expanded uncertainty is further calculated from (A.1) and (A.2).

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