Design of a Digitized Vibration Detector Implemented by CMOS Digitized Capacitive Transducer With In-Plane SoI Accelerometer

Cheng-Ta Chiang, *Senior Member, IEEE*, Chun-I Chang, and Weileun Fang, *Senior Member, IEEE*

***Abstract*— In this paper, a digitized vibration detector implemented by CMOS digitized capacitive transducer with in-plane silicon-on-insulator (SoI) accelerometer is newly proposed. The proposed digitized vibration detector is attractive due to the fact that all the circuits and the sensor can be robustly and compactly combined together. A total solution including the continuous-time-voltage (CTV) analog sensing circuits and digitalized interface are proposed in this paper. Based upon 0.35-μm 2P4M CMOS technology with 3 V power supply, all the functions and performance of the proposed CMOS digitized capacitive transducer are successfully tested and proven through measurements and confirmed it to be applied on the in-plane SoI accelerometer. The sensitivity of the proposed CTV analog sensing circuits is 50.488 mV/g and maximum nonlinearity is 2.5% over the excitation of 0.25–5.75-g intensity. The peak signal-to-noise-plus-distortion ratio of the proposed digitized vibration detector is 67.6 dB under excitation of 3.25-g intensity. The proposed digitized vibration detector is suitable for digitized accelerometer applications, such as automobiles, consumer electronics, Wii game player, and so on.**

***Index Terms*— Sensor interface, accelerometer, sensor transducer, CMOS, capacitive sensor.**

I. Introduction

NOWADAYS, MEMS (Micro Electro Mechanical Systems) accelerometers play an increasing role in applications as automobiles, navigation, vibration monitoring, and portable consumer electronics. Thus, the commercial market of accelerometers is rapidly increased. Presently, there are various accelerator designs have been reported, such as capacitance [1]–[11], piezoresistive [12], piezoelectric [13], [14], optics [15], and tunneling [16] types. For the accelerators, the corresponding readout circuits are also important. By following the characteristics of accelerators, readout circuits can be grouped into piezoelectric, piezoresistive, capacitive types, and etc. Among them, capacitive interfaces have the advantage of easily being integrated with CMOS MEMS sensors. Previous achievements related to the interface of capacitive accelerometers [17]–[32] had been demonstrated. However, sensing methods of these circuit structures are different. [17]–[22] are based on continuous-time-voltage sensing technique, and [23]–[32] are followed by switch-capacitor (SC) charge integration. Comparing these two sensing methods, the CTV sensing technique has the lower noise floor than SC charge integration [18]. Thus, analog sensing circuits of this work are wholly developed by following the CTV method. In order to consider for commercial market, a digitized output feature is also needed. The digitized output should be a bit stream, it could thus be easily sent over a wide range of transmission media, such as PSN, radio, optical, IR, ultrasonic, and etc. Besides, the sensing signal can not be easily affected by noise at low frequency band. Therefore, in order to fit to the requirements discussed above, a set of suitable CTV analog sensing circuits with digitalized interface is designed in this work. Although previous works [17]–[22] followed by the CTV method have been excellently presented, a total solution including the CTV analog sensing circuits and digitalized interface have not completely discussed yet. A table of comparisons to previously published designs is listed in Table I. Readers can understand the whole design techniques from this work, and this is the main contribution of this work.

In this work, a digitized vibration detector implemented by CMOS digitized capacitive transducer with in-plane SOI accelerometer is newly proposed. The area of the proposed CMOS digitized capacitive transducer is $1812 \times 1420\ \mu m^2$ and the power consumption including digital buffers is 18 mW. The sensitivity of the proposed CTV analog sensing circuits is 50.488 mV/g and maximum nonlinearity is 2.5% over the excitation of 0.25 to 5.75g intensity. The noise floor is 0.922 mg/Hz$^{1/2}$. The cross-axis Y sensitivity and cross-axis Z sensitivity are less than 1.7% and 1.66%, respectively. The peak signal-to-noise-plus-distortion ratio of the proposed digitized vibration detector is 67.6 dB under excitation of 3.25g intensity. The effective resolution is equal to 11 bits. The proposed digitized vibration detector is suitable for digitized accelerometer applications, such as automobiles, consumer electronics, Wii game player, etc.

In section II, the capacitive in-plane SOI accelerometer is addressed. The system architecture and simulation results are described in section III. In section IV, measurement results are

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TABLE I
COMPARISONS TO PREVIOUSLY PUBLISHED DESIGNS

	[17]	[18]	[19]	[21]	[22]	This work
Sensor Technology	Surface micromachined technology with integrated 2 μm CMOS	Surface micromachined technology with integrated 0.5 μm CMOS	0.35 μm CMOS process	0.35 μm CMOS process	0.35 μm CMOS process	SOI process
Sensing method	CTV	CTV	CTV	CTV	CTV	CTV
Sensing Range	±50 g	±6 g	±1 g	±11.5 g	±2 g	0.25-5.75g
Maximum sensitivity	N.A.	130 mV/g	520 mV/g	144 mV/g	457 mV/g	50.488 mV/g
Maximum nonlinearity	N.A.	N.A.	N.A.	N.A.	1.28%	2.5%
Whole noise floor	110 $\mu g/Hz^{1/2}$	50 $\mu g/Hz^{1/2}$	110 $\mu g/Hz^{1/2}$	130 $\mu g/Hz^{1/2}$	54 $\mu g/Hz^{1/2}$	922 $\mu g/Hz^{1/2}$
Output type	Analog	Analog	Analog	Analog	Analog	Digital

shown and discussed. Finally, section V gives conclusions and future works.

II. Capacitive In-Plane SOI Accelerometer

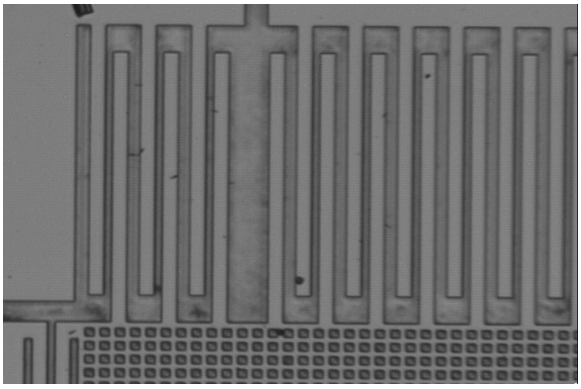
The microphotograph and measured results of the capacitive in-plane SOI accelerometer [11] are shown in Fig. 1. The measured resonant frequency is 4.987 kHz. Fabrication of MEMS devices using an SOI wafer has advantages. Firstly, it has the superior material properties due to a single crystal material. Using SOI techniques, thick devices are easily achieved. Finally, it can have less residual stresses and simple fabrication processes. The implementation of inertial sensors by using an SOI wafer has been increased [4], [6], [11], [25], [28], [30]. More detailed specification information and sensor model of the in-plane SOI accelerometer can be referred to [11]. In the section IV, the measured in-plane SOI accelerometer is experimented on the proposed CMOS digitized capacitive transducer. In the following sections, all the discussions of system architecture, simulations, and measurement results are completely discussed.

III. System Architecture and Simulation Results

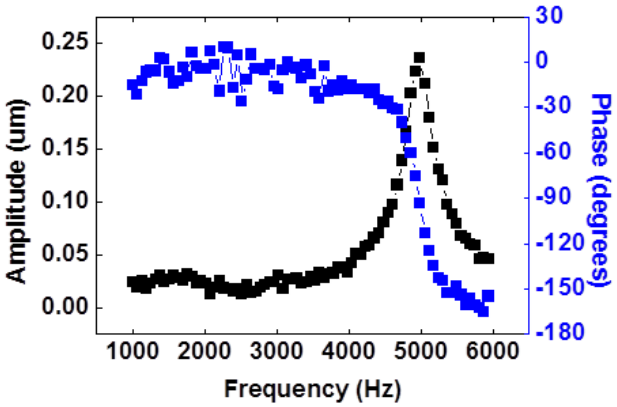
Fig. 2 shows the block diagram of the proposed CMOS digitized capacitive transducer, which consists of the capacitance to voltage converter (CVC), the demodulated chopper, Gm-C low-pass filter, gain amplifier, and the 4-stage sigma-delta modulator. All the circuit structures are discussed in this section clearly.

A. Capacitance to Voltage Converter and Gain Amplifier

According to the principle of the charge conservation, any capacitance variations will also affect the corresponding voltage value. When the vibration makes the accelerator change its capacitance, a voltage signal is generated at the same time. Based on this principle, the proposed CTV analog sensing circuits are thus designed. Fig. 3 shows the circuit



(a)



(b)

Fig. 1. The (a) microphotograph (b) measured resonant frequency of the in-plane SOI accelerometer. The resonant frequency is 4.987 kHz.

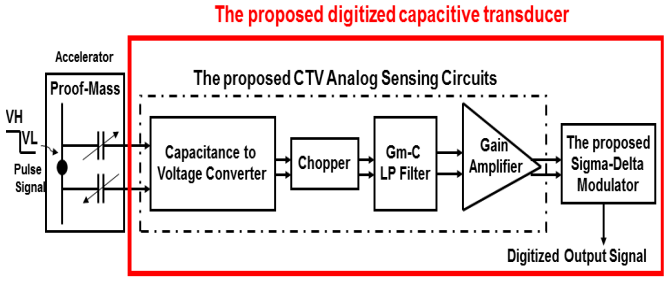


Fig. 2. The block diagram of the proposed CMOS digitized capacitive transducer.

schematic of the capacitance to voltage converter and gain amplifier. The main difference between them is the value of the capacitance C_1 and C_2. In Fig. 3(a), the C_1 is the nominal capacitance of the accelerator and C_2 is designed as a fixed capacitance of 200 fF. Due to the post-process variation, the nominal capacitance of the C_1 is generally varied between 200 to 600 fF, and the minimum and maximum capacitance of the ΔC is varied between 0.001 to 0.2% of the nominal capacitance. For the gain amplifier shown in Fig. 3(b), the C_1 and C_2 are designed 1.1 pF and 50 fF, respectively. The operational amplifier (OP) used in the CVC and gain amplifier is shown in Fig. 4. For gain amplifier, the OP performance over the frequency range from 0.1 Hz to 1 GHz is illustrated in Fig. 5. The DC gain is 72 dB, the unit gain bandwidth is 58.9 MHz, and the phase margin is 80.1°. The noise power of

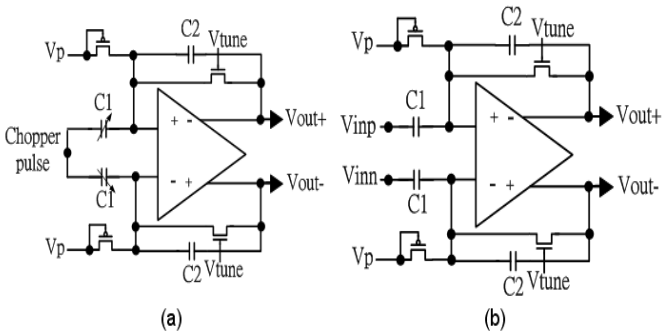


Fig. 3. The circuit schematic of the (a) capacitance to voltage converter and (b) gain amplifier.

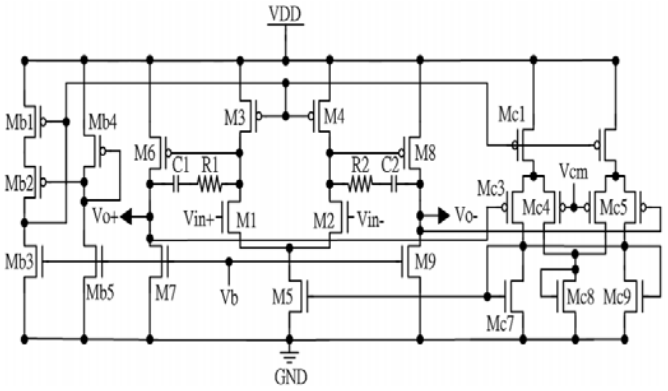
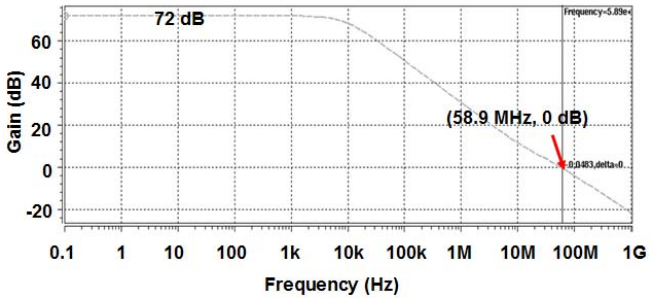
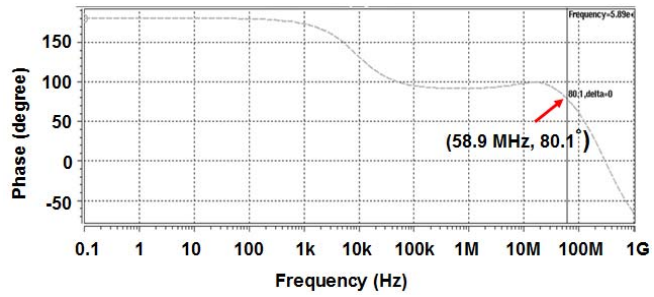


Fig. 4. The circuit schematic of the operational amplifier used in the CVC and gain amplifier.



(a)



(b)

Fig. 5. SPICE simulation results of the operational amplifier over the frequency range from 0.1 Hz to 1 GHz (a) gain and (b) phase response.

the flicker noise (1/f noise) of the OP is expressed as

$$\bar{V}n^2 = \frac{K}{C_{OX}WL}\frac{1}{f}\Delta f \qquad (1)$$

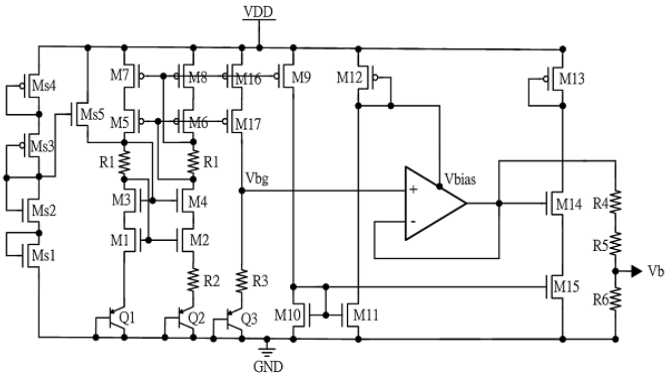


Fig. 6. The circuit schematic of the bias circuit built from the bandgap reference.

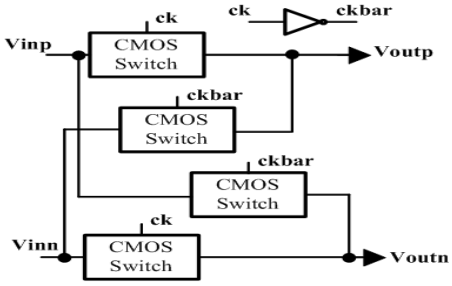


Fig. 7. The circuit schematic of the demodulated chopper.

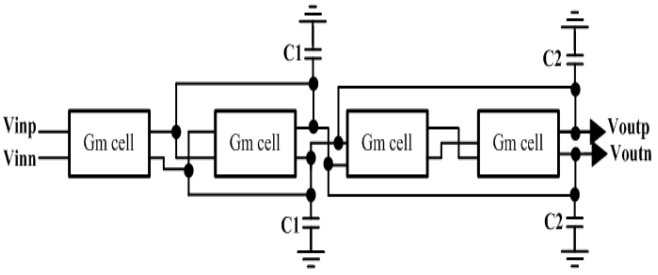


Fig. 8. The circuit schematic of the Gm-C low-pass filter.

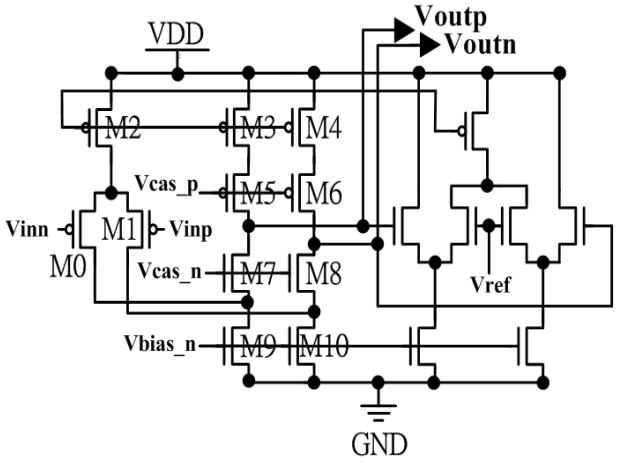


Fig. 9. The circuit schematic of the Gm cell.

where K is a process dependent constant and is on the order of 10^{-25} V^2F, C_{OX} is the capacitance per unit area of the gate oxide and is on the order of 10 fF/μm^2, and W and L are the dimensions of the transistors in the input stage. Analyzing from (1), the noise power can be reduced by making the sizes of the transistors (i.e. M_1 and M_2) larger. In the specification the resolution of the preamplifier is 10 bits. The noise needs to be less than 1 LSB. The integral noise power is expressed as

$$\sqrt{\int_{20}^{20k} \frac{K}{C_{ox}WL}\frac{1}{f}} \leq \frac{Vi}{2^{10}} \tag{2}$$

where V_i is the input signal and is on the order of 10 μV. By performing SPICE simulations, the flicker noise is integral over the frequency range from 20 Hz to 20 kHz. Thus, W and L are obtained. In order to avoid the effect of the temperature variations, the bias circuit is built with a bandgap reference and demonstrated in Fig. 6. The output voltage of the bias circuit is expressed as

$$V_b = \left(\frac{I_{16}}{I_8}\frac{R_3}{R_2}V_T * \ln n + V_{BE3}\right) * \frac{R_6}{R_4 + R_5 + R_6} \tag{3}$$

where V_T is kT/q, I_{16} and I_8 is the currents of MOS M_{16} and M_8, V_{BE3} is the base-emitter voltage of bipolar transistor (BJT) Q_3, and n is the ratio of collector currents between the BJT Q_2 and Q_1. In order to avoid interference by noise, chopping modulation principle is used. As shown in Fig. 2, the proof mass of the accelerator is chopped with a pulse signal. The sensing signal and noise at low frequency band are moved into high frequency band together. By performing the demodulated chopper as shown in Fig. 7, the sensing signal is moved into its original frequency band. However, noise remains to stay at the high frequency band. After the demodulated chopper, a low-pass filter is required to select the sensing signal and filter out the unwished signals, such as noise. The block scheme of the low-pass filter is designed with the 2nd order Gm-C structure as shown in Fig. 8. The transfer function is derived as

$$\frac{Voutn - Voutp}{Vinn - Vinp} = \frac{gm^2}{s^2C_1C_2 + sC_2gm + gm^2} \tag{4}$$

$$\omega_0 = \frac{gm}{\sqrt{C_1C_2}}, \quad Q = \sqrt{\frac{C_1}{C_2}} \tag{5}$$

where gm is the transconductance of the Gm cell demonstrated in Fig. 9, Q the quality factor of the filter, ω_0 the cut-off frequency of the filter. When the transconductance is designed well, the cut-off frequency can be easily adjusted by changing the C_1 or C_2. All the circuit blocks are integrated and grouped as the proposed CTV analog sensing circuits. In the SPICE simulations, the transient simulations of the output nodes of each analog block are demonstrated in the Fig. 10. As displayed, the sensing signal can be successfully obtained. The final close-loop gain of the proposed CTV analog sensing circuits is around 20.

B. 4-Stage Sigma-Delta Modulator

Considering digital conversion of 14 bits resolution, the design of sigma-delta modulator (SDM) is selected. Several different modulators have been used to achieve high

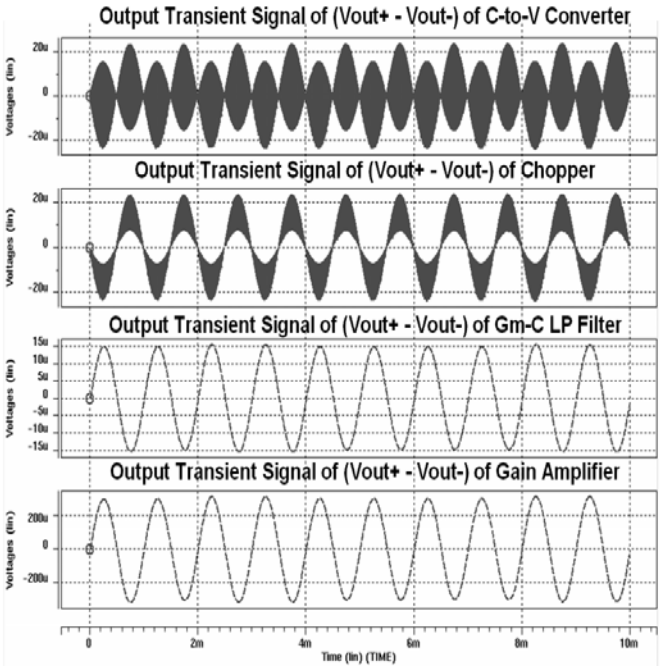


Fig. 10. SPICE transient results of the capacitance to voltage converter, chopper, Gm-C low-pass filter, and the gain amplifier. The nominal capacitance of the C_1 is 200 fF and ΔC is 2 aF. The signal frequency is 1 kHz and the chopping frequency is 200 kHz.

resolution, such as multi-loop cascade, multibit, high-order single-loop single-bit, etc [33]. In this work, a high-order single-loop single-bit architecture is chosen. The structure is attractive due to the high signal-to-noise ratio (SNR) and simple implementation. The oversampling ratio (OSR) and loop order n should be decided. For the single-bit architecture, the relationship between the dynamic range (DR) and OSR becomes

$$DR = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right) OSR^{2n+1}. \tag{6}$$

In order to consider the degradation of the achievable DR [33] and circuit non-idealities, an OSR of 256 and n of 4 are chosen.

The proposed sigma-delta modulator consists of four integrators, two analog summers, an one-bit DAC, a quantizer, and gain circuits. The gain circuits provide feedforward gain B_1 to B_4 and feedback gain G_1 as displayed in Fig. 11. The noise transfer function (NTF) of the proposed sigma-delta modulator is obtained by employing signal flow graph (SFG) and derived as

$$NTF(Z) = \frac{1}{\left\{\begin{array}{l} 1 + A_1B_1\left(\frac{1}{Z-1}\right) + (A_3A_4G_1 + A_1A_2B_2)\left(\frac{1}{Z-1}\right)^2 \\ +(A_1A_3B_1B_4G_1 + A_1A_2A_3B_3)\left(\frac{1}{Z-1}\right)^3 \\ +(A_1A_2A_3A_4B_4 + A_1A_2A_3A_4B_2G_1)\left(\frac{1}{Z-1}\right)^4 \end{array}\right\}} \tag{7}$$

where A_1, A_2, A_3, A_4, B_1, B_2, B_3, B_4, and G_4, are coefficients of the proposed sigma-delta modulator. With

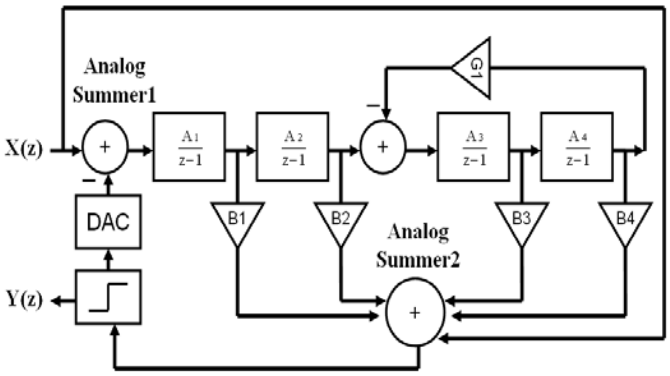


Fig. 11. The topology of the proposed sigma-delta modulator for the digitized capacitive transducer.

careful filter design, a Butterworth high-pass NTF is obtained as

$$NTF_{\text{butterworth}}(Z) = \frac{1}{\left\{\begin{array}{l} 1 + 0.0583\left(\frac{1}{Z-1}\right) + 0.2687\left(\frac{1}{Z-1}\right)^2 \\ +0.0672\left(\frac{1}{Z-1}\right)^3 \\ +0.0051\left(\frac{1}{Z-1}\right)^4 \end{array}\right\}} \tag{8}$$

By using MATLAB to perform the behavior simulations of the $NTF_{butterworth}$ (Z), the poles of the $NTF_{butterworth}$ (Z) are all located inside the unit circle, which are $0.8167 \pm 0.4804i$ and $0.8912 \pm 0.044i$. Thus, it analyzes in ensuring stability. By mapping (7) and (8), the coefficients of A_1, A_2, A_3, A_4, B_1, B_2, B_3, B_4, and G_4 are 0.166, 0.35, 0.25, 0.1, 5, 4.6, 3.8, 3.4, and 0.0166, respectively. The circuit implementations of the proposed sigma-delta modulator is built and demonstrated in Fig. 12. The entire circuit is implemented in switched-capacitor (SC) networks. In the modulator, the OP is the main building block which determines the main performance and consumes most of the current of the whole circuits. The folded-cascaded OP shown in Fig. 13 is designed. The SC common-mode feedback (SC CMFB) is used due to its simplicity and efficiency in current consumption. To avoid signal dependent charge injection, non-overlapping clock signals are used. Instead of OP-based analog summer, the SC-based analog summer can reduce power consumption, and the circuit is implemented as shown in Fig. 14(a). Besides, the quantizer is displayed in Fig. 14(b). SPICE simulations are performed to obtain the output codes of the proposed sigma-delta modulator. These digital codes are used to calculate the signal-to-noise-plus-distortion ratio (SNDR) of the modulator through dedicated MATLAB programs. The dedicated programs are to perform fast Fourier transform (FFT) from these obtained codes. These codes are to calculate the signal power and noise power from the FFT data, and finally are to calculate the value of the SNDR. After performing MATLAB simulations, Fig. 15 shows the SNDR versus the input signal level. The DR is 98 dB and the peak SNDR is 86.1 dB. The effective resolution is equal to 14 bits, which is calculated as $(86.1-1.76)/6.02 = 14$ bits.

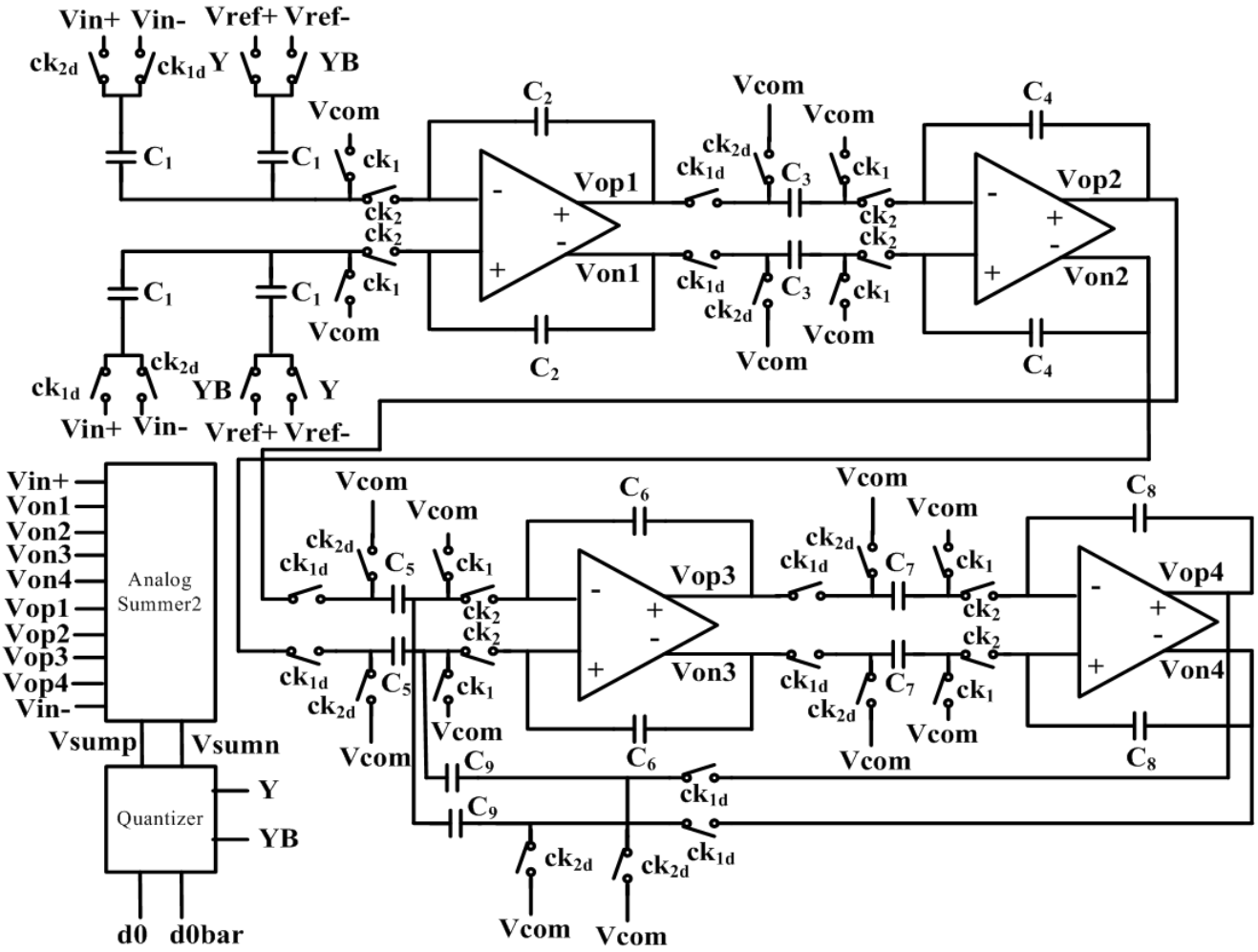


Fig. 12. The whole circuit schematic of the proposed sigma-delta modulator.

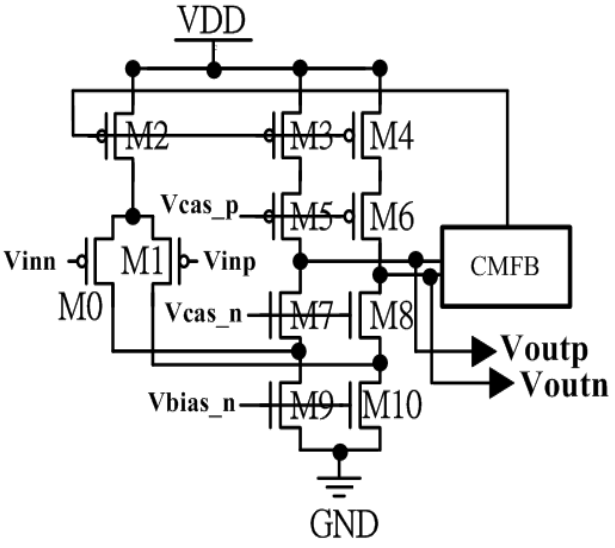


Fig. 13. The circuit schematic of the folded-cascaded OP used in the proposed sigma-delta modulator.

C. The Whole System

All the circuit blocks are integrated into the proposed digitized vibration detector. The output signals of the proposed CTV analog sensing circuits are inputted into the 4-stage delta-sigma modulator. In Fig. 16, the peak SNDR is around 69.2 dB under the nominal capacitance of the C_1 of 600 fF and ΔC of 1.2 fF. The signal frequency is 1 kHz and the chopping frequency is 200 kHz. The effective resolution is equal to 11.2 bits. All the functions and performance of the proposed digitized vibration detector are successfully tested and proven through SPICE simulations.

IV. Measurement Results

Fig. 17 demonstrates the physical layout and microphotograph of the proposed CMOS digitized capacitive transducer. The area of the proposed CMOS digitized capacitive transducer is $1812 \times 1420\ \mu\text{m}^2$ and the power consumption including digital buffers is 18 mW. Fig. 18 shows the proposed digitized vibration detector and measurement setup. The measurement setup includes power supplies, a LDS V40B electrodynamic shaker, a Tektronix-TDS1012B oscilloscope, a Tektronix-3022B signal generator, an Agilent-33522A function generator, an Agilent-35670 dynamic signal analyzer, and the proposed chip. Firstly, the shaker is excited by the signal generator. In the measurement, the frequency of shaker is fixed at 100 Hz. The function generator is used to

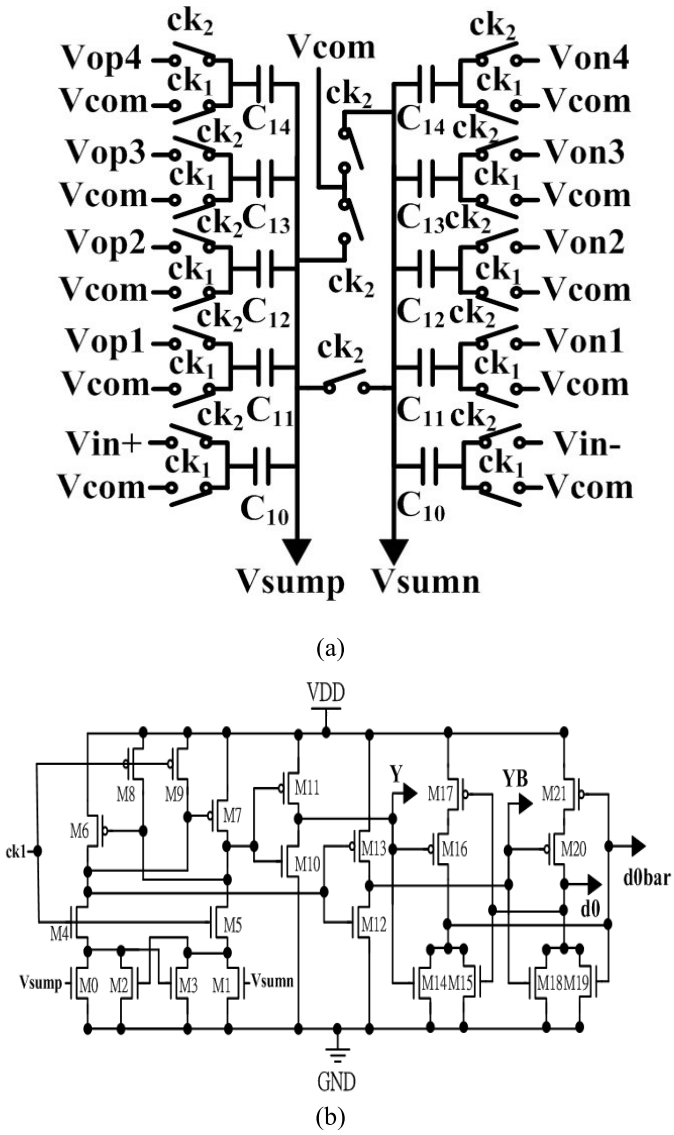


Fig. 14. The circuit schematic of (a) analog summer and (b) quantizer.

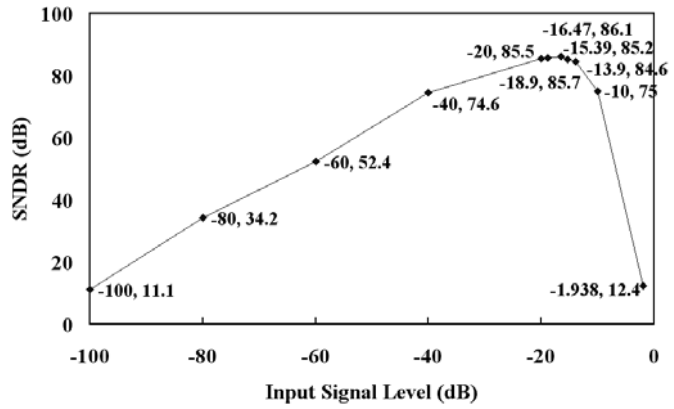


Fig. 15. The SNDR versus input signal level.

generate the chopping frequency and the sampling frequency. The chopping and sampling frequency are fixed at 200 kHz and 5 MHz, respectively. The dynamic characteristic of the shaker is also monitored by a commercial accelerometer

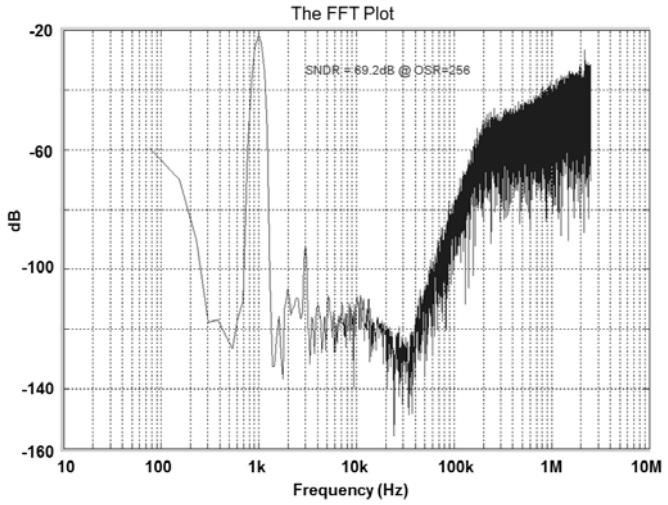


Fig. 16. The output spectrum of the proposed digitized vibration detector. The nominal capacitance of the C_1 is 600 fF and ΔC is 1.2 fF. The signal frequency is 1 kHz and the chopping frequency is 200 kHz.

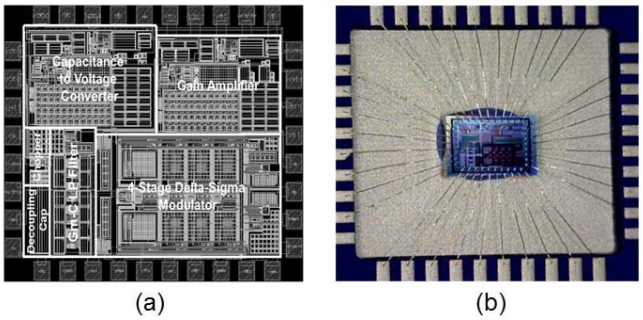


Fig. 17. The (a) physical layout and (b) microphotograph of the proposed CMOS digitized capacitive transducer.

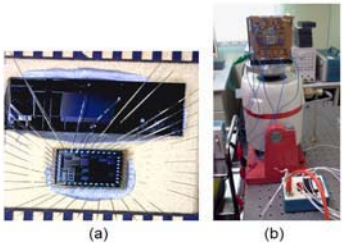
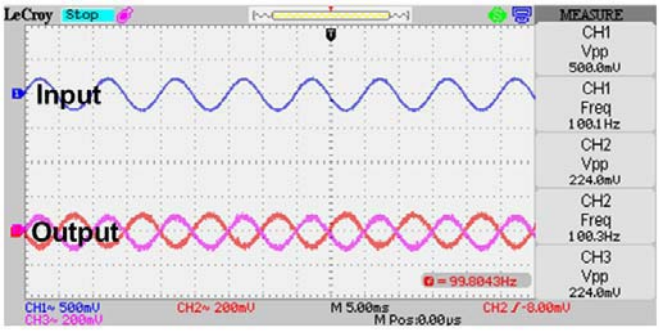
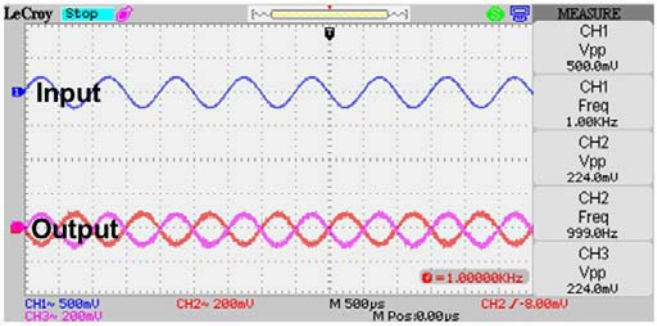


Fig. 18. (a) The proposed digitized vibration detector and (b) the measurement setup.

PCB-J352C34. After exciting the shaker, the sensing signal of the proposed digitized vibration detector is measured to analyze the transient and frequency response. The transient responses of the reference accelerometer and the proposed CTV analog sensing circuits with excitation of 2.5g intensity are shown in Fig. 19, respectively. The upper waveform is the output of reference accelerometer, and the lower waveform is the output of the proposed CTV analog sensing circuits. Measured results of digitized stream output with excitation of 2.5g intensity are displayed in Fig. 20. As proven, the digitized stream output is correctly pulse-density modulated. In Fig. 21, the frequency response is measured under excitation of 1g intensity. As displayed, the capacitance variations of the in-plane SOI accelerometer are successfully

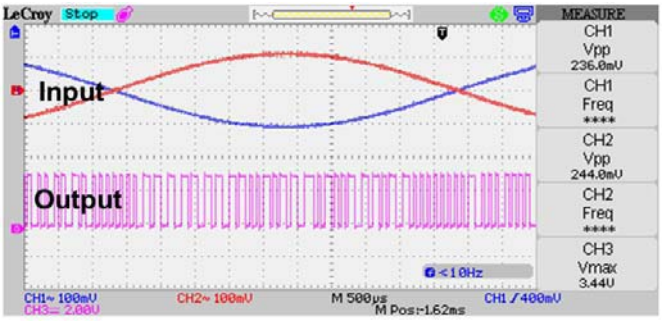


(a)

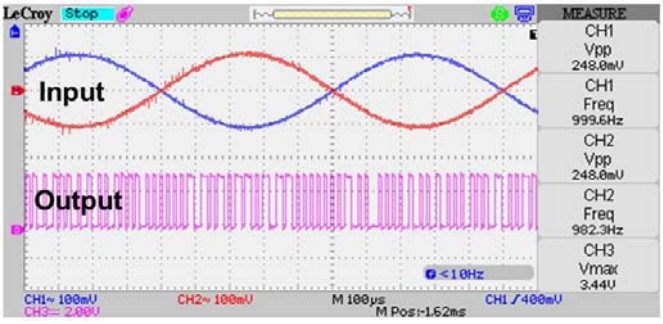


(b)

Fig. 19. The transient response of the reference accelerometer and the proposed CTV analog sensing circuits with excitation of 2.5 g intensity. The frequency of shaker is (a) 100 Hz and (b) 1 kHz.



(a)



(b)

Fig. 20. Measured results of digitized stream output with excitation of 2.5 g intensity. The frequency of shaker is (a) 100 Hz and (b) 1 kHz.

converted into voltage variations by the proposed TV analog sensing circuits. All the measured outputs of the proposed CTV analog sensing circuits are plotted in Fig. 22. The

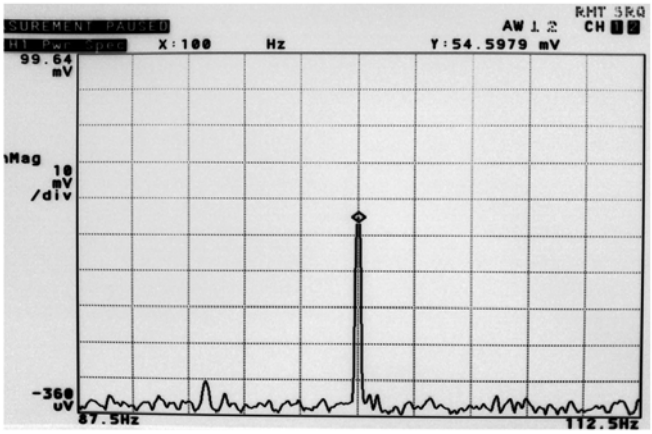


Fig. 21. The frequency response of the proposed digitized vibration detector. The frequency of shaker is 100 Hz and is also with excitation of 1g intensity.

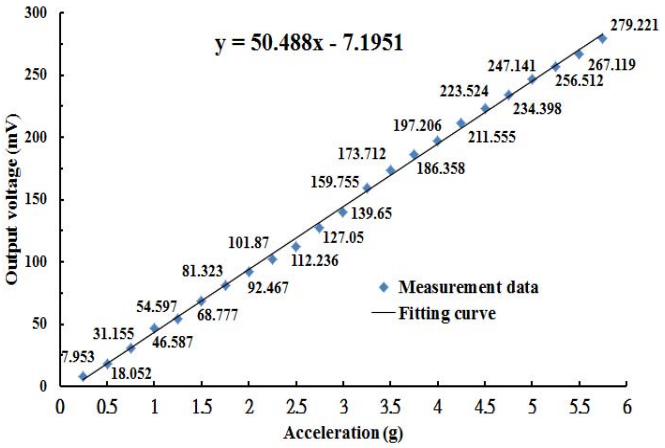


Fig. 22. The sensitivity of the proposed digitized vibration detector under shaking frequency of 100 Hz and excitation of 1g intensity.

sensitivity is 50.488 mV/g over the excitation of 0.25 to 5.75g intensity. In addition, the noise floor is determined from [11]

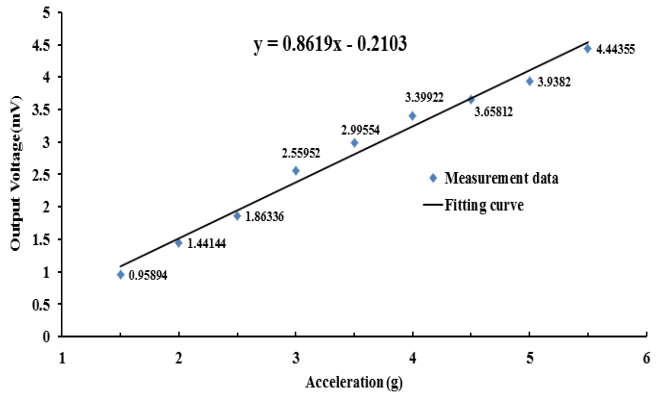
$$Noise\ floor = \frac{output\ noise}{sensitivity} \times \left(\frac{1}{\sqrt{bandwidth}}\right) \quad (9)$$

where the output noise and the bandwidth are measured by the dynamic signal analyzer. The output noise and bandwidth are 46.56 μV and 1 Hz, respectively. By (9), the noise floor is 0.922 mg/Hz$^{1/2}$. Moreover, maximum nonlinearity is derived as [34]

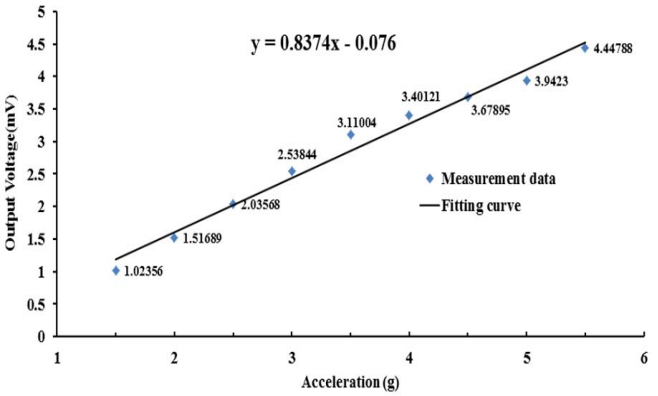
$$Maximum\ non\text{-}linearity = \frac{maximum\ deviation\ (V)}{full\ scale\ output\ (V)} \times 100\%. \quad (10)$$

By (10), maximum nonlinearity is 2.5% over the excitation of 0.25 to 5.75g intensity. In Fig. 23, the cross-axis sensitivities in the Y-axis and Z-axis are measured under excitation of 1g intensity. The cross-axis Y sensitivity and cross-axis Z sensitivity are less than 1.7% and 1.66%, respectively.

Finally, measured results of the peak SNDR of the proposed digitized vibration detector are shown in Fig. 24. The peak



(a)



(b)

Fig. 23. The cross-axis (a) Y and (b) Z sensitivity of the proposed digitized vibration detector under shaking frequency of 100 Hz and excitation of 1 g intensity.

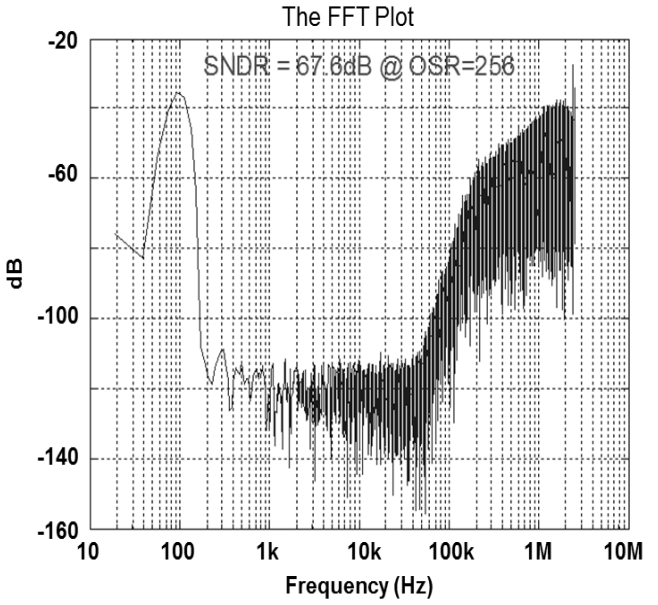


Fig. 24. Measured results of the peak SNDR of the proposed digitized vibration detector. The peak SNDR is 67.6 dB under shaking frequency of 100 Hz and excitation of 3.25g intensity.

SNDR is 67.6 dB under excitation of 3.25g intensity. The effective resolution is 11 bits. Compared with simulation results in section II, the effective resolution is almost the same. That implies that the proposed CMOS digitized capacitive transducer and in-plane SOI accelerometer are robustly and compactly combined together. Thus, all the functions and performance between simulations and measurements can successfully match each other. Compared with [17]–[22], the output type of this work is digital. However, the whole noise floor of this work is higher than other works. That is because more back-end signal processing circuits are added in this work. Thus, more noise coming from circuits must be also generated. Although the sensitivity of this work is not as large as previous works, it can be adjusted by the gain of gain amplifier. The characteristics of the proposed CMOS digitized vibration detector are summarized in Table II.

TABLE II
SUMMARY ON THE CHARACTERISTICS OF THE PROPOSED DIGITIZED VIBRATION DETECTOR

Technology	0.35 μm CMOS 2P4M
Power supply	3.0 V
Power consumption	18 mW
Chopping frequency	200 kHz
Sampling frequency	5 MHz
OSR	256
Measured signal bandwidth	<10 kHz
Measured range	0.25-5.75 g
Sensitivity	50.488 mV/g
Maximum nonlinearity	2.5%
Maximum cross-axis Y sensitivity	1.7%
Maximum cross-axis Z sensitivity	1.66%
Noise floor	0.922 mg/$Hz^{1/2}$
Measured peak SNDR of the proposed chip with Z-axis SOI accelerometer	67.6 dB @ 3.25g
Physical layout area	1812 × 1420 μm^2
Application field	Micro-accelerometers

V. CONCLUSION

A digitized vibration detector implemented by CMOS digitized capacitive transducer with in-plane SOI accelerometer is newly proposed. All the functions and performance of the proposed CMOS digitized vibration detector are successfully tested and proven through measurements. The core functionalities of the proposed digitized vibration detector are successfully obtained and may be applied to the automobiles and consumer products. In the future, the developed techniques are adaptively designed into digitized accelerometer applications.

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REFERENCES

[1] H. Qu, D. Fang, and H. Xie, "A single-crystal silicon 3-axis CMOS-MEMS accelerometer," in *Proc. IEEE Sensors Conf.*, Oct. 2004, pp. 661–664.

[2] H. Takao, Y. Matsumoto, H. See, and M. Ishida, "A monolithically integrated three-axis accelerometer using CMOS compatible stress-sensitive differential amplifiers," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 109–116, Jan. 1999.

[3] B. Chen, J. Miao, C. K. Lim, F. E. H. Tay, and C. Iliescu, "Dynamic behavior of high-G MEMS accelerometer incorporated with novel micro-flexures," *Int. J. Softw. Eng. Knowl. Eng.*, vol. 15, no. 2, pp. 225–230, Apr. 2005.

[4] H. Takao, Y. Matsumoto, H. See, M. Ishida, and T. Nakamura, "Analysis and design considerations of three-dimensional vector accelerometer using SOI structure for wide temperature range," *Sens. Actuators A, Phys.*, vol. 55, nos. 2–3, pp. 91–97, Jul. 1996.

[5] C. M. Sun, M. H. Tsai , Y. C. Liu, and W. Fang, "Implementation of a monolithic single proof-mass tri-axis accelerometer using CMOS-MEMS technique," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1670–1679, Jul. 2010.

[6] K. I. Lee, H. Takao, K. Sawada, and M. Ishida, "Low temperature dependence three-axis accelerometer for high temperature environments with temperature control of SOI piezoresistors," *Sens. Actuators A, Phys.*, vol. 104, no. 1, pp. 53–60, Mar. 2003.

[7] C. Iliescu and J. Miao, "One-mask process for silicon accelerometers on Pyrex glass utilising notching effect in inductively coupled plasma DRIE," *Electron. Lett.*, vol. 39, no. 8, pp. 658–659, Apr. 2003.

[8] L. M. Roylance and J. B. Angell, "A batch-fabricated silicon accelerometer," *IEEE Trans. Electron Devices*, vol. 26, no. 12, pp. 1911–1917, Dec. 1979.

[9] C.-K. Chan, S.-C. Lo, Y.-C. Huang, M. Wu, M.-Y. Wang, and W. Fang, "Poly-Si based two-axis differential capacitive-sensing accelerometer," *IEEE Sensors J.*, vol. 12, no. 12, pp. 3301–3308, Dec. 2012.

[10] M.-H. Tsai, Y.-C. Liu, and W. Fang, "A three-axis CMOS-MEMS accelerometer structure with vertically integrated fully differential sensing electrodes," *J. Microelectromech. Syst.*, vol. 21, no. 6, pp. 1329–1337, Dec. 2012.

[11] C.-P. Hsu, M.-C. Yip, and W. Fang, "Implementation of a gap-closing differential capacitive sensing Z-axis accelerometer on an SOI wafer," *J. Micromech. Microeng.*, vol. 19, no. 7, pp. 1–7, Jul. 2009.

[12] A. Partridge, J. K. Reynolds, B. W. Chui, E. M. Chow, A. M. Fitzgerald, L. Zhang, *et al.*, "A high-performance planar piezoresistive accelerometer," *J. Microelectromech. Syst.*, vol. 9, no. 1, pp. 58–66, Mar. 2000.

[13] B. Puers and W. Sansen, "A new uniaxial accelerometer in silicon based on the piezojunction effect," *IEEE Trans. Electron Devices*, vol. 35, no. 6, pp. 764–770, Jun. 1988.

[14] P. Scheeper, J. O. Gulloy, and M. Kofoed, "A piezoelectric triaxial accelerometer," *J. Micromech. Microeng.*, vol. 6, no. 1, pp. 131–133, 1996.

[15] T. Storgaard-Larsen, S. Bouwstra, and O. Leistiko, "Optomechanical accelerometer based on strain sensing by a Bragg grating in a planar waveguide," *Sens. Actuators A, Phys.*, vol. 52, nos. 1–3, pp. 25–32, Apr. 1996.

[16] C. H. Liu, A. M. Barzilai, J. K. Reynolds, A. Partridge, T. W. Kenny, J. D. Grade, *et al.*, "Characterization of a high-sensitivity micromachined tunneling accelerometer with micro-G resolution," *J. Microelectromech. Syst.*, vol. 7, no. 2, pp. 235–244, Jun. 1998.

[17] M. Lemkin and B. E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 456–468, Apr. 1999.

[18] J. Wu, G. K. Fedder, and L. R. Carley, "A low-noise low-offset capacitive sensing amplifier for 50-$\mu g/\sqrt{Hz}$ monolithic CMOS MEMS accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 722–730, May 2004.

[19] H. Qu, D. Fang, and H. Xie, "A monolithic CMOS-MEMS 3-axis accelerometer with a low-noise, low-power dual-chopper amplifier," *IEEE Sensors J.*, vol. 8, no. 9, pp. 1511–1518, Sep. 2008.

[20] K. T. C. Chai, D. Han, R. P. Singh, D. D. Pham, C. Y. Pang, J. W. Luo, *et al.*, "118-dB dynamic range, continuous-time opened-loop capacitance to voltage converter readout for capacitive MEMS accelerometer," in *Proc. Asian Solid-State Circuits Conf.*, Nov. 2010, pp. 1–4.

[21] H. Sun, D. Fang, K. Jia, F. Maarouf, H. Qu, and H. Xie, "A low-power low-noise dual-chopper amplifier for capacitive CMOS-MEMS accelerometers," *IEEE Sensors J.*, vol. 11, no. 4, pp. 925–933, Apr. 2011.

[22] S. S. Tan, C. Y. Liu, L. K. Yeh, Y. H. Chiu, M. S. C. Lu, and K. Y. J. Hsu, "An integrated low-noise sensing circuit with effect bias stabilization for CMOS MEMS capacitive accelerometers," *IEEE Trans. Circuits Syst., I, Reg. Papers*, vol. 58, no. 11, pp. 2661–2672, Nov. 2011.

[23] C. Lu, M. Lemkin, and B. E. Boser, "A monolithic surface micromachined accelerometer with digital output," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1367–1373, Dec. 1995.

[24] H. Kulah, J. Chae, N. Yazdi, and K. Najafi, "A multi-step electromechanical $\Delta\Sigma$ converter for micro-g capacitive accelerometers," in *Proc. IEEE ISSCC*, Feb. 2003, pp. 202–203.

[25] B. V. Amini and F. Ayazi, "A 2.5-V 14-bit $\Sigma\Delta$ CMOS SOI capacitive accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2467–2476, Dec. 2004.

[26] V. P. Petkov and B. E. Boser, "A fourth-order $\Sigma\Delta$ interface for micromachined inertial sensors," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1602–1609, Aug. 2005.

[27] H. Kulah, J. Chae, N. Yazdi, and K. Najafi, "Noise analysis and characterization of a sigma-delta capacitive microaccelerometer," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 352–361, Feb. 2006.

[28] B. V. Amini, R. Abdolvand, and F. Ayazi, "A 4.5-mW closed-loop micro-gravity CMOS SOI accelerometer," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2983–2991, Dec. 2006.

[29] M. Paavola, M. Kämäräinen, J. A. M. Järvinen, M. Saukoski, M. Laiho, and K. A. I. Halonen, "A micropower interface ASIC for a capacitive 3-axis micro-accelerometer," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2651–2665, Dec. 2007.

[30] L. He, Y. P. Xu, and M. Palaniapan, "A CMOS readout circuit for SOI resonant accelerometer with 4-μg bias stability and 20-$\mu g/\sqrt{Hz}$ resolution," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1480–1490, Jun. 2008.

[31] M. Yücetas, M. Pulkkinen, A. Kalanti, J. Salomaa, L. Aaltonen, and K. Halonen, "A high-resolution accelerometer with electrostatic damping and improved supply sensitivity," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1721–1730, Jul. 2012.

[32] Z. Ye, H. Yang, T. Yin, G. Huang, and F. Liu, "High-performance closed-loop interface circuit for high-Q capacitive microaccelerometers," *IEEE Sensors J.*, vol. 13, no. 5, pp. 1425–1433, May 2013.

[33] R. Schreier and G. C. Temes, *Understanding Delta-sigma Data Converters*. New Work, NY, USA: IEEE Press, 2004.

[34] *AN012 Accelerometer Errors* [Online]. Available: http://www.kionix.com/sites/default/files/AN012%20Accelerometer%20Errors.pdf

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