

PAPER

## Implementation of various vacuum conditions in sealed chambers for wafer-level bonding by using embedded cavity

To cite this article: C-W Cheng *et al* 2017 *J. Micromech. Microeng.* **27** 015002

View the [article online](#) for updates and enhancements.

### Related content

- [Realize multiple hermetic chamber pressures for system-on-chip process by using the capping wafer with diverse cavity depths](#)  
Shyh-Wei Cheng, Jui-Chun Weng, Kai-Chih Liang *et al.*
- [Tube-shaped Pirani gauge for in situ hermeticity monitoring of SiN thin-film encapsulation](#)  
F Santagata, J F Creemer, E Iervolino *et al.*
- [Removable fast package technology for MEMS devices](#)  
Chia-Min Lin, Wen-Chih Chen and Weileun Fang

### Recent citations

- [Enhancing airtightness of TGV through regulating interface energy for wafer-level vacuum packaging](#)  
Yunbin Kuang *et al*
- [Surface activated room-temperature bonding in Ar gas ambient for MEMS encapsulation](#)  
Hideki Takagi *et al*
- [Realize multiple hermetic chamber pressures for system-on-chip process by using the capping wafer with diverse cavity depths](#)  
Shyh-Wei Cheng *et al*



**IOP | ebooks™**

Bringing you innovative digital publishing with leading voices to create your essential collection of books in STEM research.

Start exploring the collection - download the first chapter of every title for free.

# Implementation of various vacuum conditions in sealed chambers for wafer-level bonding by using embedded cavity

C-W Cheng<sup>1,2</sup>, K-C Liang<sup>2</sup>, C-H Chu<sup>1</sup> and W Fang<sup>2</sup>

<sup>1</sup> Taiwan Semiconductor Manufacturing Company (TSMC) Ltd, Hsinchu, Taiwan

<sup>2</sup> Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan

E-mail: [fang@pme.nthu.edu.tw](mailto:fang@pme.nthu.edu.tw)

Received 30 May 2016, revised 25 September 2016

Accepted for publication 30 September 2016

Published 25 October 2016



## Abstract

The existing foundry processes enable the fabrication and integration of various sensors on a single chip. However, various vacuum conditions of these sensors remain a critical concern after packaging. For example, accelerometers and gyroscopes are operated under two different vacuum conditions. This study extends the concept of using outgassing to realize sealed chambers under different vacuum conditions in one wafer-level bonding step. In other words, by etching various numbers and sizes of cavities on a substrate, the vacuum condition of a sealed chamber can be modulated. In applications, resonators and Pirani gauges were fabricated and characterized to demonstrate the feasibility of the proposed process scheme. The vacuum condition of the sealed chambers was then monitored using the quality factor (detected by resonators) and the pressure (measured by Pirani gauges). The measurements indicate that the sealed chambers with vacuum conditions ranging from approximately 2 to 180 mbar were simultaneously fabricated and integrated on the same wafer. This approach could facilitate the monolithic integration of devices with different vacuum requirements, such as approximately 100 mbar chamber pressure for accelerometers, and single-digit millibars vacuum conditions for gyroscopes.

Keywords: chamber pressure, vacuum condition, embedded cavity

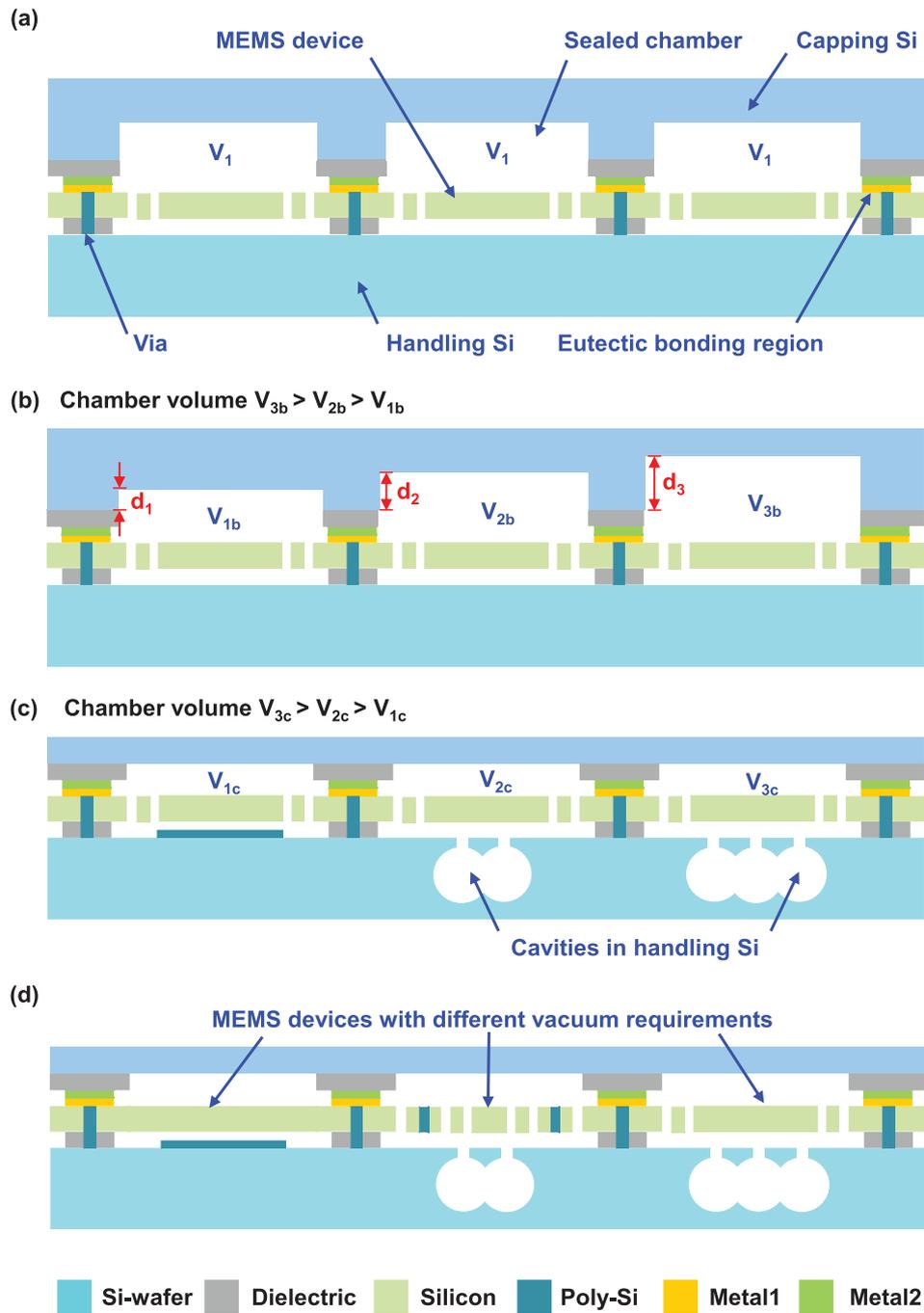
(Some figures may appear in colour only in the online journal)

## 1. Introduction

Motion sensors such as accelerometers, gyroscopes, magnetometers, and altimeters are extensively applied in wearable devices. To meet the requirements of different applications, a combination of these motion sensors together with a sensing algorithm was demonstrated [1]. In addition to single sensing devices, combo sensors comprising various sensors have attracted attention. In general, combo sensors can be achieved using numerous approaches, including SoC (system on chip) and SiP (system in package). Reducing the process efforts for combo sensors is an important consideration for foundries and IDMs (integrated device manufacturers). Therefore, various process platforms have been developed and are commercially available for foundries (e.g. the THELMA platform

of ST Microelectronics [2], the BOSCH platform [3], the Si above CMOS (complementary metal-oxide semiconductor) of TSMC (Taiwan Semiconductor Manufacturing Company) [4], and the Tronics platform [5]. In addition, various process platforms have been demonstrated in research organizations, such as the CMOS-MEMS (micro electro mechanical systems) platform [6, 7], the M&NEMS (nano electro mechanical systems) 'generic' platform of Leti [8], and the SiGe MEMS platform of imec [9, 10]. The processes for implementing MEMS devices by integrating CMOS and SOI (silicon on insulator) technologies have been investigated in [11, 12], and a review of various approaches of heterogeneous integration of MEMS and IC has also been reported in [13].

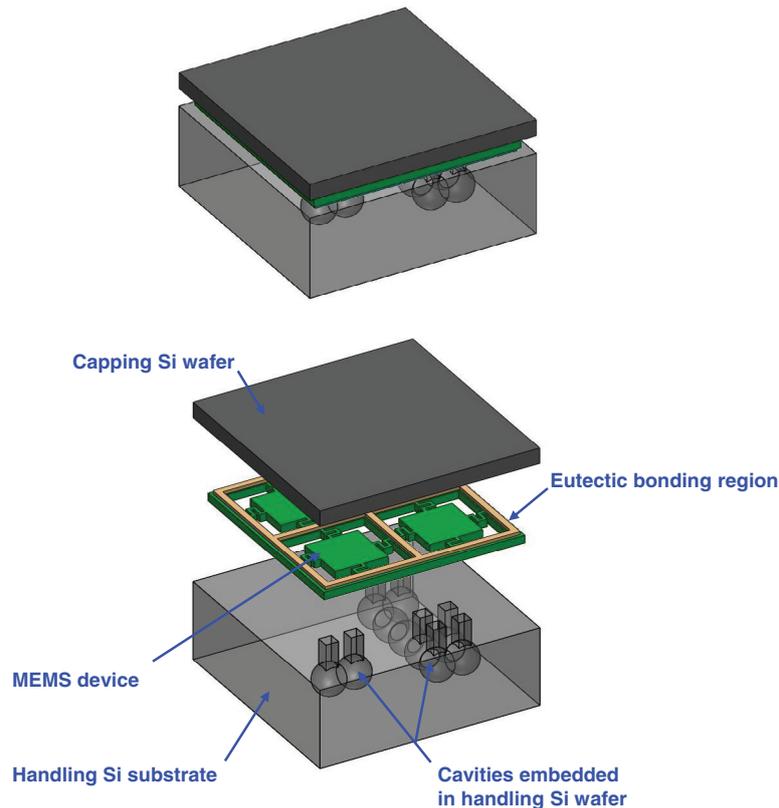
The process scheme established in [4] provides an effective manufacturing and integration solution for motion sensors.



**Figure 1.** (a) and (b) The existing approach to modulating the vacuum condition of sealed chambers by varying the chamber depth of the capping wafer. (c) Proposed approach for modulating the vacuum condition of sealed chambers by etching the cavities on the substrate under the suspended device. The vacuum condition is modulated by the size and number of the cavities. (d) Devices with various vacuum conditions are monolithically fabricated and integrated using the process scheme and further sealed through wafer-level bonding.

Suspended MEMS structures with a uniform thickness were implemented using a Si layer. The integration approach offers the shortest interconnect between the MEMS devices and CMOS chips. The process scheme was further improved to meet various requirements such as the thermal budget [14]. In addition to motion sensors, the aforementioned technique is appropriate for fabricating resonant MEMS devices. Although the fabrication and integration problems have been solved using the process scheme, the vacuum conditions after packaging remain critical challenges. For example, air damping

(i.e. low vacuum) is required for accelerometers [15], whereas a high quality factor (i.e. high vacuum) is required for gyroscopes and resonant devices [16]. Consequently, the characteristics of outgassing from thin films [17, 18] have been demonstrated for low-vacuum devices. On the basis of the process scheme in [1, 4], a few approaches have been reported for enabling the monolithic integration of the MEMS devices to meet various vacuum requirements [19, 20]. Sealed and unsealed chambers can be fabricated using the process reported in [20]. The vacuum condition of a sealed chamber



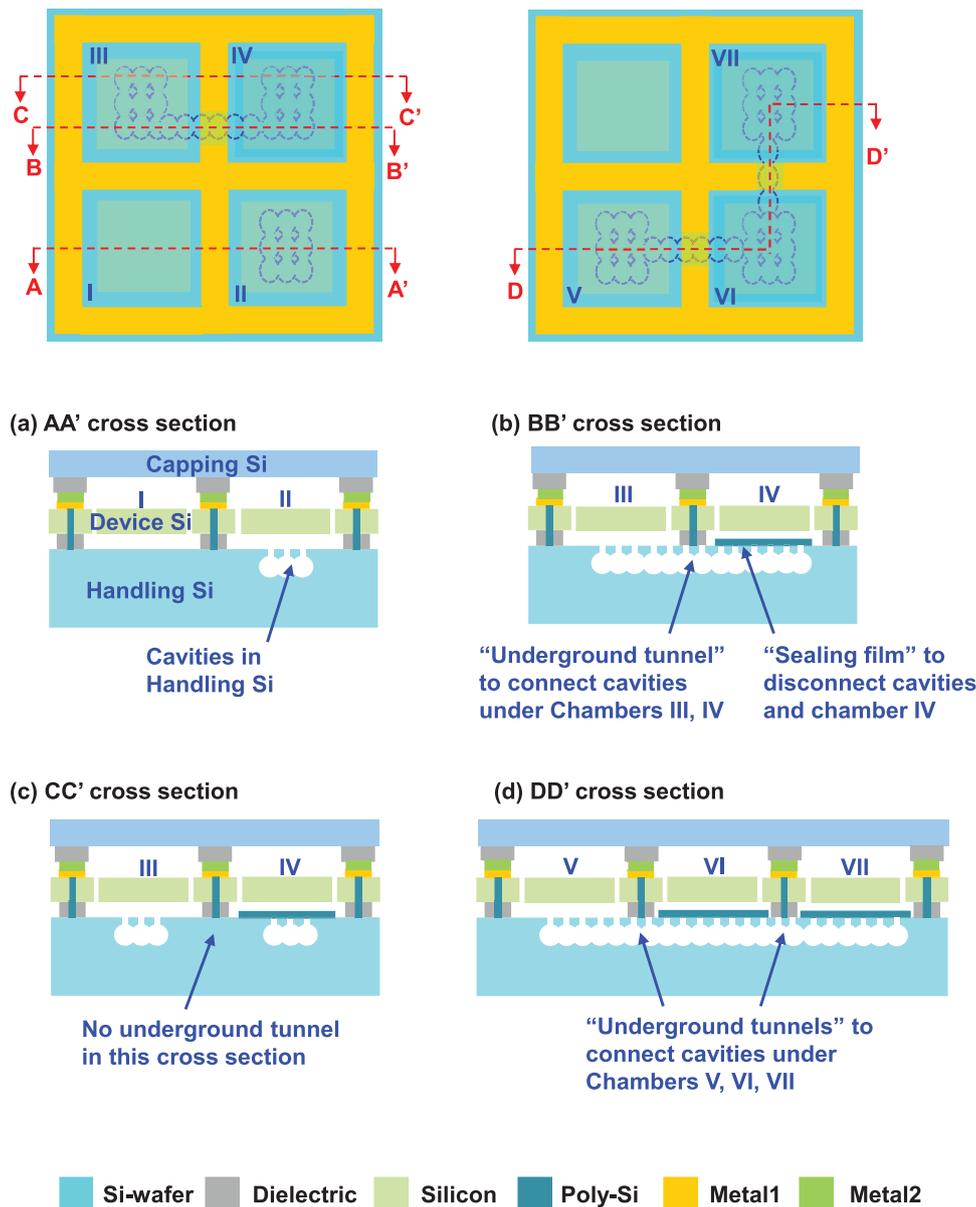
**Figure 2.** Architecture of the monolithically integrated and packaged devices with various vacuum conditions. The sensing chip consists of the capping wafer, suspended MEMS structure, and substrate with various cavities.

is determined by the bonding process, whereas the vacuum condition of an unsealed chamber is equal to the ambient conditions. Moreover, as demonstrated in [20], the bulk-Si Pirani vacuum gauge can be monolithically realized and integrated in the process. Thus, the *in situ* monitoring of the vacuum conditions of a packaged chip is achieved.

As reported in [19], the outgassing characteristics can be exploited to modulate the vacuum conditions of a sealed chamber. However, multiple etching processes are required to define the various depths on a cap wafer. Moreover, a large chamber volume entails a large etching depth on the cap wafer, which causes a major design concern regarding the structural rigidity. The present study further extended the concept in [19] to achieve various vacuum conditions in one wafer-level bonding step. The sealed chamber volume was modulated by varying the number and size of the etching cavities on the substrate. The resonators and Pirani gauges were fabricated and characterized to demonstrate the feasibility of the proposed process scheme. The pressure measured using the Pirani gauge and the quality factor of the resonator were exploited to monitor the vacuum condition of the sealed chambers. The experiments demonstrated that the chambers with high (single digit millibars) to low (a few tens to over a hundred millibars) vacuum conditions were simultaneously fabricated and integrated on the same wafer using the proposed process scheme. This approach could enable monolithic integration of devices with various vacuum requirements (e.g. more than 100 mbar for accelerometers, and single digit millibars for gyroscopes).

## 2. Design concepts and fabrication process

In this study, the design concept was based on a commercially available MEMS process scheme shown in figure 1(a). As indicated in the figure, a thin single crystal silicon (Si) layer was bonded on top of the Si substrate with a dielectric spacer. The suspended MEMS structures were defined and implemented using a thin Si layer. Moreover, another Si layer was used to serve as the capping for the newly fabricated MEMS devices. The process scheme offers a simple approach to fabricate MEMS devices and further monolithically integrate these devices on a single chip. It is a potential process platform for realizing inertial sensors and gyroscopes as a motion sensing hub. However, in this process scheme, the air pressure in each sealed MEMS device is the same as the ambient pressure during bonding. Therefore, no substantial difference in the quality factor between the MEMS devices under the same level of air damping was observed. This is a critical concern for the monolithic integration of devices with various requirements for dynamic responses, such as accelerometers and gyroscopes. The characteristics of outgassing from dielectric layers were employed in [19], which enabled the sealed chambers to exhibit various vacuum levels. According to the equation of state for an ideal gas, the air pressure and damping coefficient of the sealed device can be modulated by varying the volume of the chamber. As shown in figure 1(b), the volume of the sealed chamber was changed by varying the etching depths of the capping wafer. For example, the

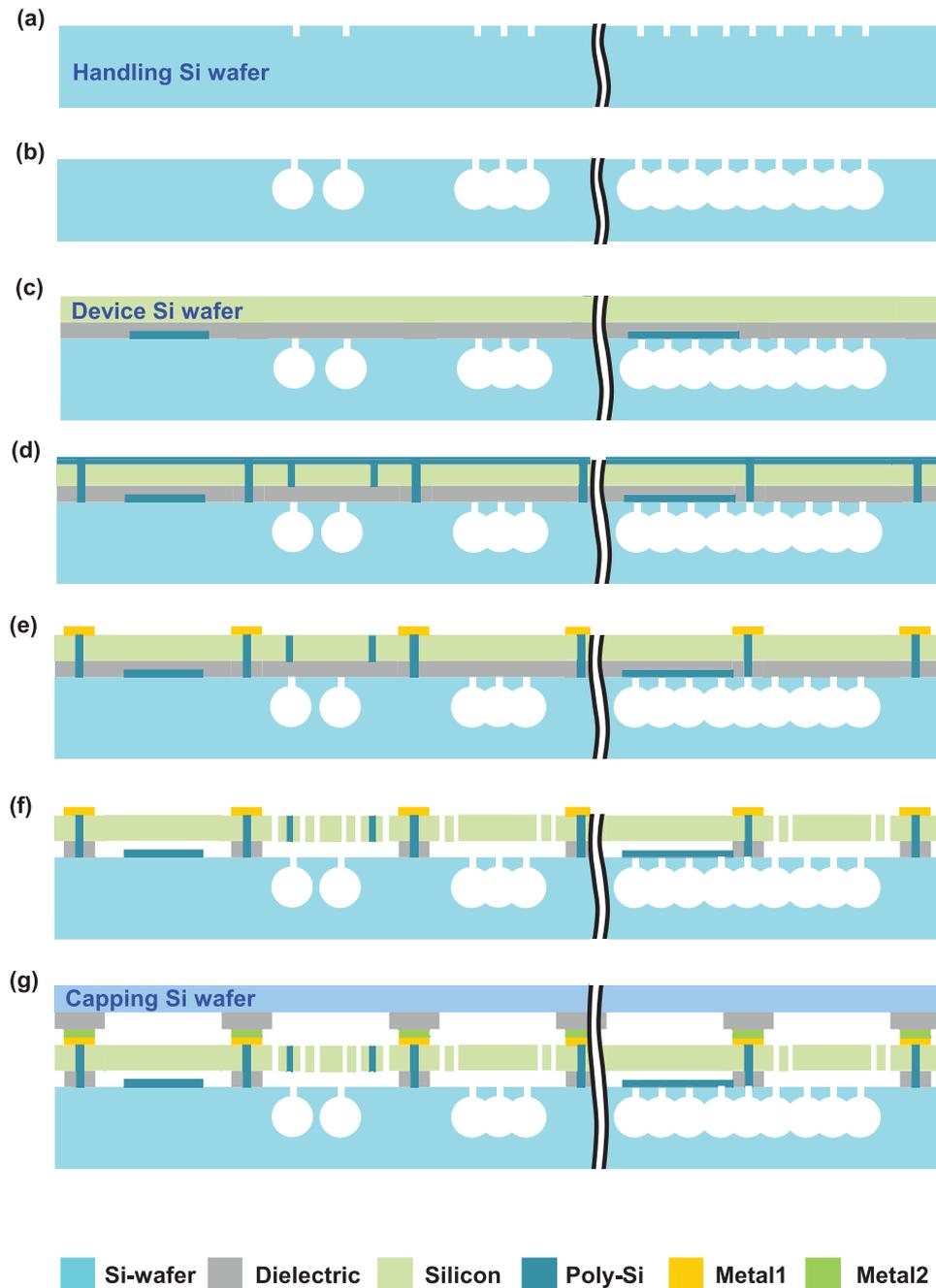


**Figure 3.** Schematic of the various vacuum conditions of the sealed chambers modulated by the cavity arrangements. (a) Chambers with and without cavities. (b) The cavities in chamber III are connected to chamber IV through an ‘underground tunnel’ to further enhance the volume of chamber III. Note that the cavities in chamber IV are sealed using a ‘sealing film’. (c) The decrease in the structural rigidity must be reduced during the arrangement of underground tunnel. (d) Cavities under devices V–VII can also be connected through the underground tunnel to further increase the volume of chamber V.

etching depths  $d_3 > d_2 > d_1$  will lead to a volume difference of  $V_{3b} > V_{2b} > V_{1b}$ . However, the decrease in the mechanical stiffness of the capping wafer could be problematic when increasing the depth of the largest cavity for vacuum improvement. For example, cracks could be induced in the capping wafer during the thinning-down process. These cracks could then lead to leakage problems and breakage of the capping wafer. Therefore, increasing the thickness of the capping wafer to improve its stiffness is more effective. However, the Z-axis form factor would be increased. Another option is to increase the footprint of the capping wafer; however, this may lead to increased device costs. The present study proposed a design concept, shown in figure 1(c), to fabricate auxiliary cavities on the Si substrate. The chamber volume of each sealed device is

varied with the number and size of the cavities. For example, the volume difference of  $V_{3c} > V_{2c} > V_{1c}$  in the figure mainly resulted from the number of embedded cavities. On the basis of the proposed process scheme, monolithic implementation of various packaged devices with various ambient pressures (i.e. damping coefficients) is possible using wafer-level processing. As indicated in figure 1(d), a gyroscope that requires a high vacuum environment is packaged in the chamber with volume  $V_{3c}$ , whereas an accelerometer that requires sufficient air damping is sealed in the chamber with volume  $V_{1c}$ .

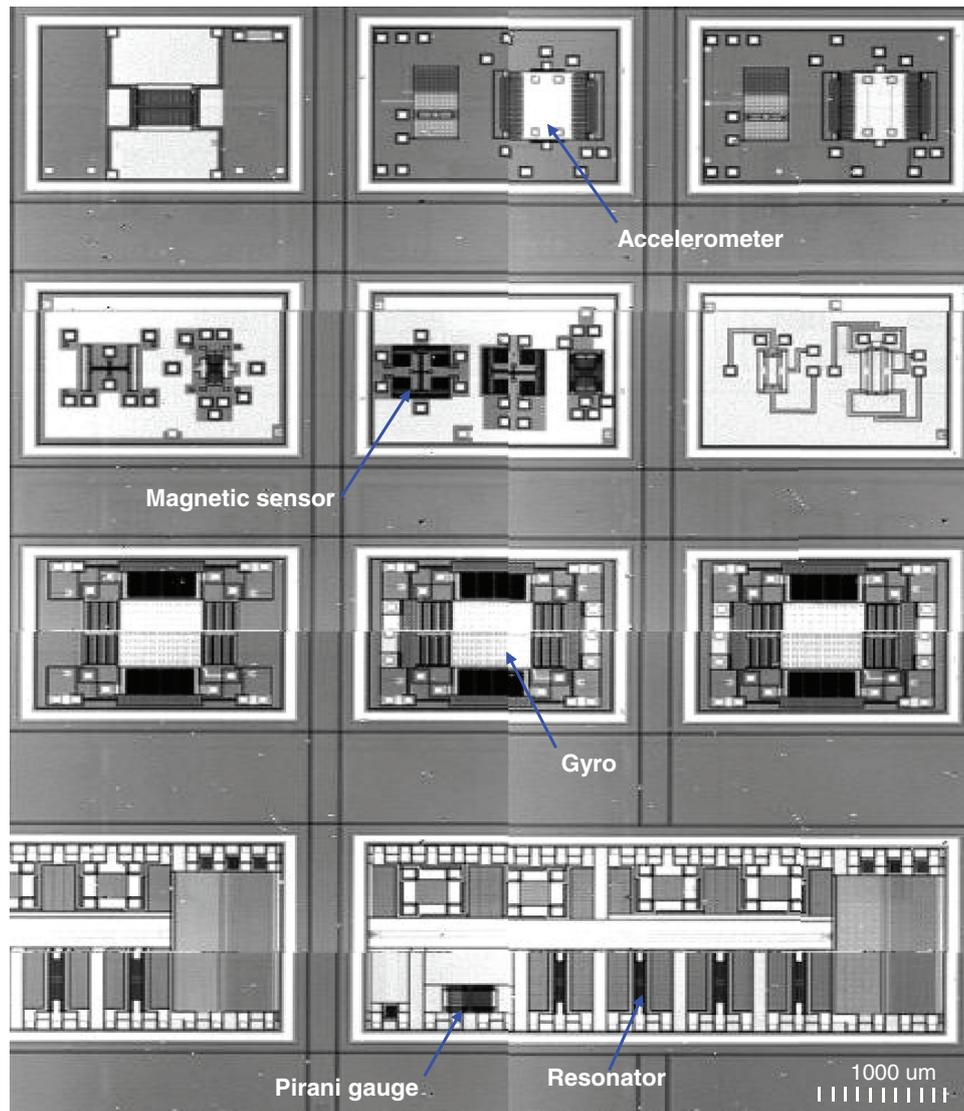
Figure 2 illustrates the detailed design of the proposed concept. The sensing chip was monolithically integrated with four sensors with the capping wafer, suspended MEMS devices, and handling substrate. The present study exploited



**Figure 4.** Fabrication process steps: (a) the Si substrate was patterned using DRIE to define the location of the cavities; (b) the Si isotropic etching was used to define the cavities on the substrate; (c) the handling Si substrate was fusion bonded with a device Si wafer comprising patterned SiO<sub>2</sub> and poly-Si layers. The bonding surface of the device Si wafer was polished using CMP to enhance the bonding quality. The device Si wafer was thinned down after bonding to define the MEMS structure thickness. (d) The device Si layer was etched using DRIE and then filled with a CVD poly-Si film to form poly-plugs; (e) The poly-Si film was patterned to realize the poly-plugs, and a metal film was deposited and patterned for the subsequent eutectic bonding. (f) The device Si layer was patterned using DRIE to define the MEMS structures, and the oxide film was removed using vapor HF to release the MEMS devices from the Si substrate. (g) The wafer-level eutectic bonding process was used to hermetically seal the suspended MEMS devices.

the handling substrate under the suspended MEMS structures to create cavities to enlarge the air chamber. According to the equation of state for an ideal gas, at a given outgassing condition, the volume of the air chamber and the vacuum condition are determined by the number and size of the cavities. Moreover, the number and size of the cavities are defined by the fabrication processes. Because the outgassing condition is known in advance, the number and size of the

cavities as well as the vacuum condition are predictable and can be considered as the design parameters. Furthermore, figure 3 illustrates some possible designs to vary the volume of the air chambers. The cross section AA' in figure 3(a) shows the integration of two devices with various ambient pressure requirements. Both chamber I (without cavities) and chamber II (with cavities) are sealed after bonding. After the outgassing from thin films, the sealed chamber I

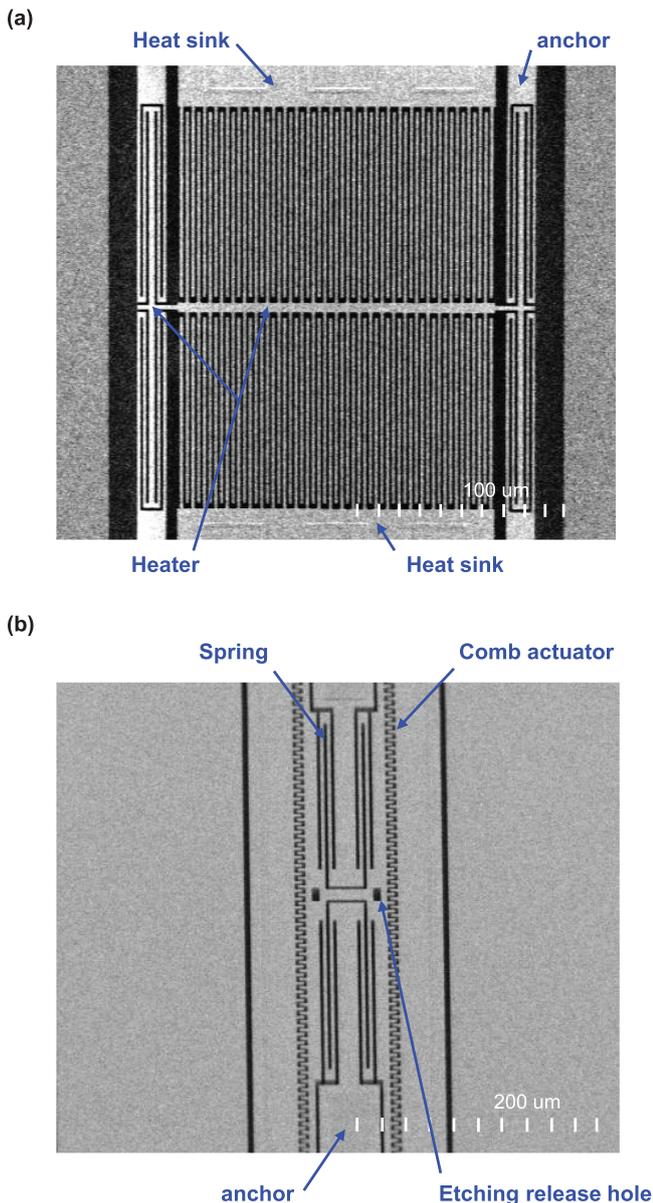


**Figure 5.** Stitching of optical micrographs showing typical results of fabricating various devices on a single fabricated chip by using the proposed process scheme.

(for device I) is in a relatively low vacuum environment compared with the sealed chamber II (for device II). Moreover, according to the study design, the substrate underneath the sealed chambers could be connected to further increase the chamber volume, as shown by the cross section BB' in figure 3(b), which indicates that the cavities in chamber III and chamber IV are connected through an 'underground tunnel'. The cavities in chamber IV are sealed using a bonded film (the details about sealing cavities by using a bonded film are explained in the process steps), and thus chamber IV and the cavities underneath are not connected. Consequently, all the substrate cavities underneath devices III and IV only contribute to the volume enhancement of chamber III, thereby enabling packaged devices with two different vacuum conditions. Notably, only a few cavities are arranged under the bonding area to prevent a decrease in stiffness, as shown in cross section CC' of figure 3(c). In addition, to prevent the effect on device rigidity, the cavity

is not placed around the device anchor area. Similarly, the cross section DD' in figure 3(d) shows that the substrate underneath devices V–VII (and vice versa) could also be employed to modulate the ambient chamber pressure of the packaged devices. The vacuum condition of sealed chamber V can be further improved by increasing the number of cavities. In summary, these substrate cavities are connected through the underground tunnel to circumvent the bonding ring without damaging the bonding quality and hermetic seal property of each chamber. This flexible arrangement that provides extra space for vacuum improvement during the integration of multiple sensors is an additional advantage of the proposed design.

Figure 4 illustrates the steps of the established process scheme. As shown in figure 4(a), the bare handling Si substrate was anisotropically etched using DRIE (deep reactive ion etching) to define the locations of the cavity. As shown in figure 4(b), Si isotropic etching was used to define the



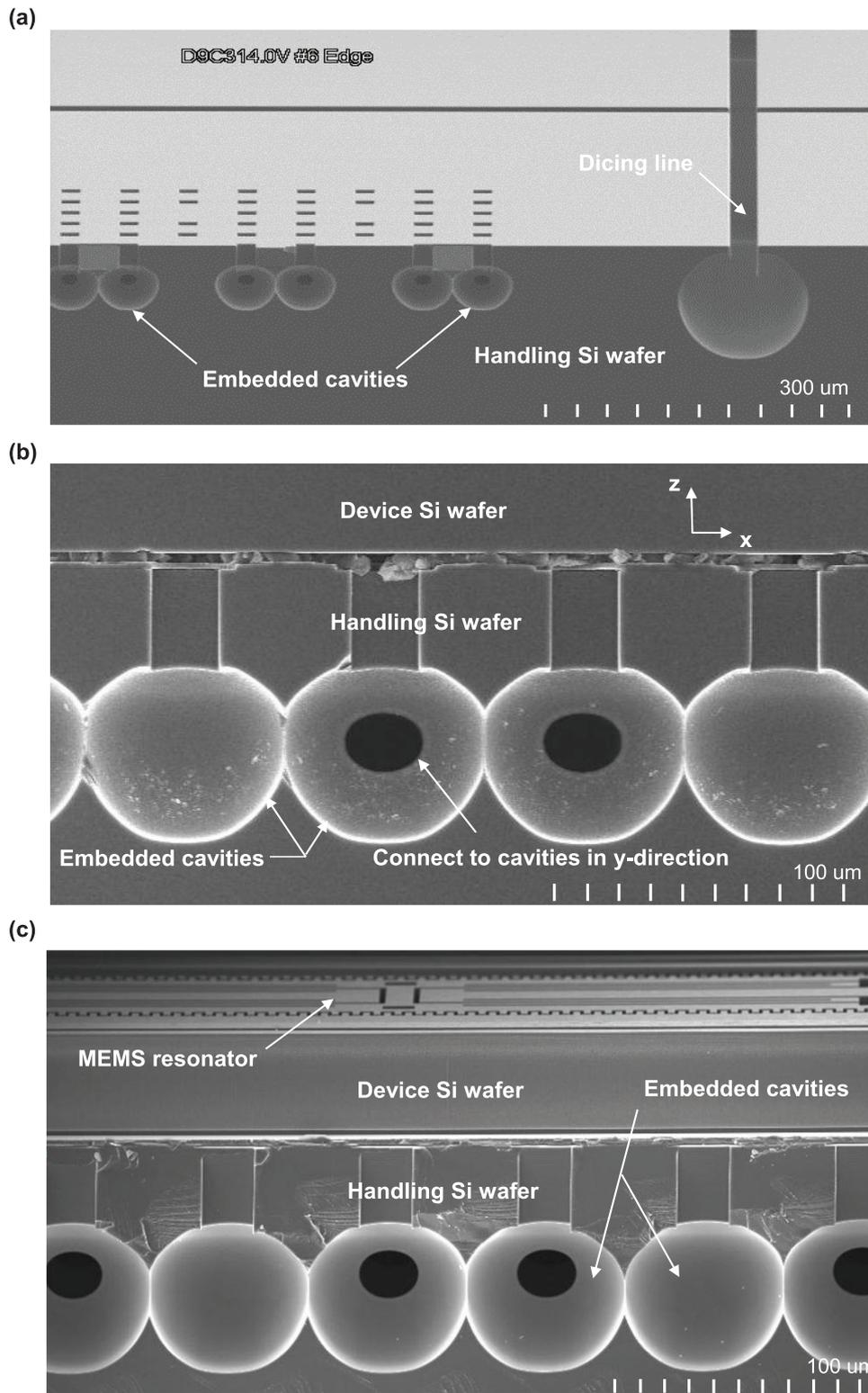
**Figure 6.** Close-up SEM micrographs of the two sensors revealing information regarding the characterization of the vacuum conditions of sealed chambers: (a) Pirani gauge, and (b) resonator.

embedded cavities on the substrate. The size of the cavities was defined by the etching time.  $\text{SiO}_2$  was used to protect the substrate surface and the sidewalls of the DRIE holes during the Si isotropic etching. The steps in figures 4(a) and (b) are similar to part of the SCREAM (single crystal reactive etching and metallization) process [21]. As shown in figure 4(c), the complete handling Si substrate was fusion bonded with another device Si wafer with patterned  $\text{SiO}_2$  and poly-Si layers. The bonding surface of the device Si wafer was polished using CMP (chemical mechanical polishing) to enhance the quality of fusion bonding. Subsequently, the thinning process was performed on the device Si wafer to define the thickness of the MEMS structures. As illustrated in figure 4(d), the device Si layer was etched using DRIE to

define the location and shape of the poly-plugs. The poly-Si film was deposited through CVD (chemical vapor deposition) to fill the etching holes and then patterned to realize the poly-plugs. A metal film was then deposited and patterned for the subsequent eutectic bonding. As shown in figure 4(e), DRIE was employed to define the MEMS structures on the device Si layer. Moreover, the oxide film deposited on the device Si wafer (figure 4(c)), which served as the sacrificial layer, was removed using vapor HF (hydrofluoric acid) to release the MEMS devices from the Si substrate. Finally, as illustrated in figure 4(f), the wafer-level eutectic bonding process (Al–Ge eutectic bonding with a temperature range between 400 °C and 450 °C) was performed to hermetically seal the suspended MEMS devices (using Si or CMOS wafers). The volume of the sealed chamber is highly dependent on the size and number of the embedded cavities. Therefore, chambers with different volumes ( $V_{1c}$ ,  $V_{2c}$ , and  $V_{3c}$ ) were implemented, as indicated in figure 1(c). In addition, the sealed chamber with an extra-large volume  $V_{4c}$  was realized by connecting the cavities under two devices using the underground tunnel.

### 3. Experiment results and discussion

The stitching of the optical micrographs in figure 5 demonstrates the typical fabrication results of the process scheme (without capping). The results indicate that various sensors with different vacuum requirements, including accelerometers, resonators, and resonant type magnetometers, were monolithically implemented using the process scheme. Moreover, ambient pressure monitoring sensors such as Pirani gauges were also realized using the process. The close-up scanning electron microscope (SEM) micrographs in figure 6 reveal more detailed information about the built-in Pirani gauge and resonator for characterizing the vacuum conditions of the sealed chambers. The SEM micrographs in figure 7 display the cavities etched on the substrate to augment the volume of air chambers. The micrograph in figure 7(a) displays the cavities implemented through isotropic etching after the process shown in figure 4(b). The micrograph in figure 7(b) depicts a device Si layer that was bonded to the substrate with cavities and with the interface sacrificial  $\text{SiO}_2$  before removal, as shown in figure 4(c). The isotropically etched cavities could be clearly observed on the close-up SEM micrograph. These cavities were connected to each other in the horizontal direction (i.e. the in-plane  $x$ -axis direction, as marked on the micrograph). In other words, these cavities formed a single air chamber. The volume of the air chamber can be modulated by varying the size and number of these isotropically etched cavities. Moreover, as indicated in the micrograph, the central dark area is connected to the cavity along the in-plane  $y$ -axis direction. The distribution of cavities in the in-plane  $x$ -axis and  $y$ -axis directions demonstrates that the proposed design could offer a wide space for air chambers and vacuum modulation. Furthermore, the micrograph in figure 7(c) displays the cavities embedded in the substrate underneath a patterned MEMS device. This device was associated with the

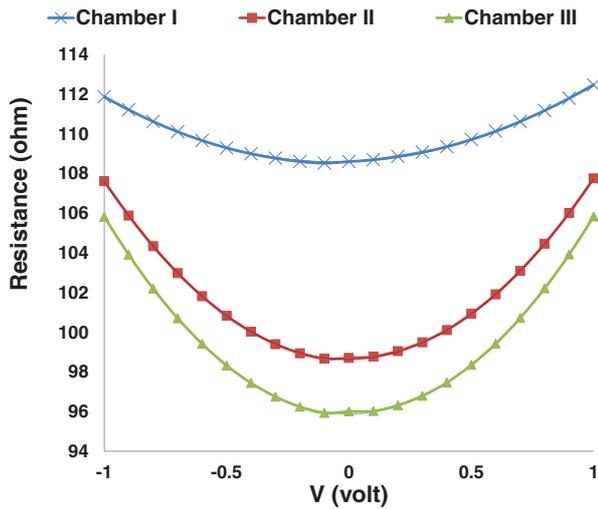


**Figure 7.** (a) Cavities implemented through isotropic etching after the process shown in figure 4(b). (b) The device Si layer is bonded to the substrate with cavities, and the interface sacrificial SiO<sub>2</sub> has not yet been removed, as in the process shown in figure 4(c). (c) A bonded device Si layer is etched using DRIE process on the top of the substrate with cavities, at the same process step shown in figure 4(f).

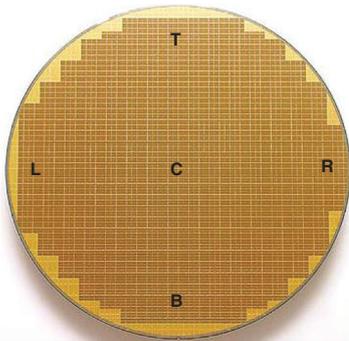
process step shown in figure 4(f); however, the vapor HF release process was not yet performed at this stage to etch away the interface sacrificial SiO<sub>2</sub>.

To monitor the pressure of the sealed chamber after the bonding of capping wafer, this study fabricated Pirani gauges

and resonators by using the process scheme described in [14,22]. These devices are presented in figure 6. Pressures ranging from 0.1 to 1013 mbar can be monitored by the fabricated Pirani vacuum gauge. Figure 8 presents typical measurement results from the Pirani gauges embedded in three chambers



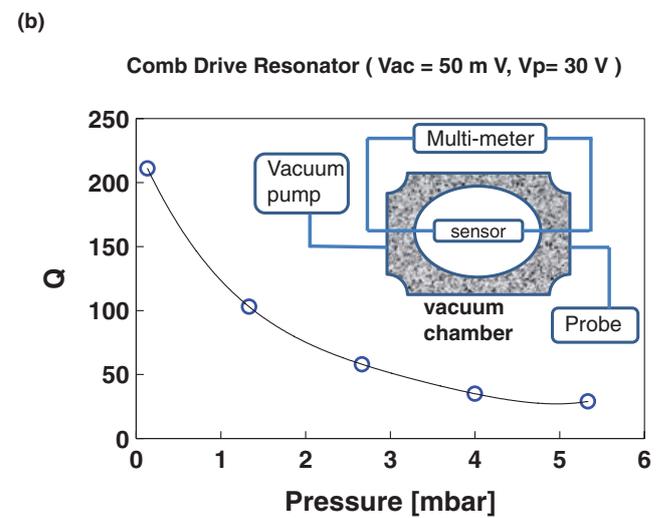
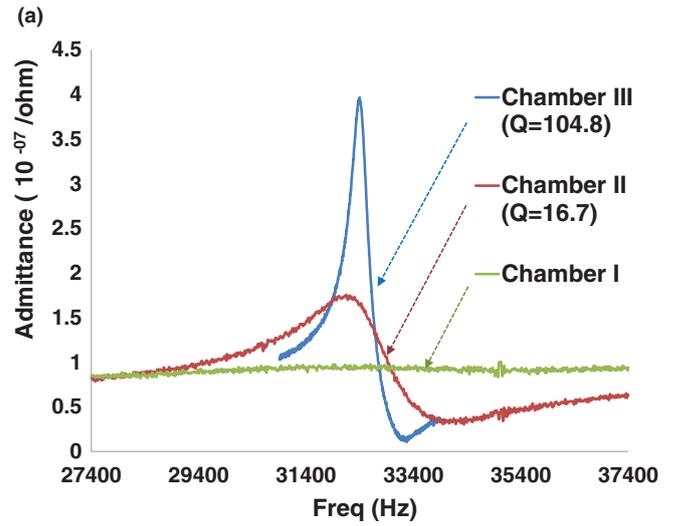
**Figure 8.** Typical resistance-voltage curves measured using Pirani gauges from three sealed chambers with various cavities. Chamber I contains no cavity, and chambers II and III contain 28 and 850 cavities, respectively. These devices are located on the chip in the central region of the wafer.



Location \ Pressure (unit : m bar)	C	R	L	T	B
Chamber I	180.4	130.6	196.2	169.0	178.8
Chamber II	83.3	39.2	87.3	73.0	88.1
Chamber III	2.2	1.1	2.7	2.2	3.1

**Figure 9.** Correlated pressure distribution map of the wafer. Three sealed chambers are measured using Pirani gauges distributed at five regions of the wafer (C, center; L, left; R, right; T, top; and B, bottom).

with various numbers of cavities. Chamber III contained more than 850 embedded cavities with a volume of approximately  $5.5 \times 10^7 \mu\text{m}^3$ , chamber II contained 28 embedded cavities with a volume of approximately  $2.2 \times 10^6 \mu\text{m}^3$ , and chamber I contained no embedded cavity. The distributions of the embedded cavities in chambers I–III are displayed in figures 3(a) and (b). According to [21], the measured voltage-resistance curves could be fitted using the following second-order polynomial equation to determine the pressure coefficient  $C_2$ :



**Figure 10.** (a) Measured dynamic responses of resonators sealed in chambers with various cavities. The quality factors in various sealed chambers are also determined. (b) Calibration of the resonator quality factor at various ambient pressures.

$$y = C_2x^2 + C_1x + C_0. \tag{1}$$

Furthermore, the thermal impedance and chamber pressure were determined. The chamber pressures associated with the measurements in figure 8 were 2.2, 83.3, and 180.4 mbar, respectively. The results demonstrated that the proposed approach can be used to successfully modulate the pressure of the sealed chambers by varying the number of cavities on the substrate. The pressure of the sealed chambers distributed at various locations in the wafer was also calibrated in this study. The measurements shown in figure 9 summarize the pressure distribution of the sealed chambers on an 8 inch wafer. In addition, the locations of these chambers are marked on the image of the entire wafer (C, center; L, left; R, right; T, top; and B, bottom). Note that the results in figure 8 were measured from the central region. The results in figure 9 depict that the chamber pressures at different locations have

reasonable uniformity except the 'R' region. By excluding the results of the 'R' region, the variation in chamber pressure was 4%–19% for the high-vacuum chamber (chamber I with low pressure), 1%–13% for the mid-vacuum chamber (chamber II with medium pressure), and 1%–8% for the low-vacuum chamber (chamber III with high pressure). According to the results in figure 9, the pressure ratios between chambers II and III ranged from 28 to 37. Moreover, the volume ratio between chambers II and III was 1/25. Thus, the results indicate a good correlation between chamber volume and pressure. Moreover, the electrostatic comb-drive resonators were fabricated and capped in chambers of three vacuum conditions (also modulated by cavity numbers). Figure 10(a) presents the typical frequency responses measured from the resonators sealed in different chambers. Similarly, chamber I contained no embedded cavity, and chambers II and III contained 28 and 850 embedded cavities, respectively. The quality factors of the resonators sealed in high vacuum and medium vacuum were 104.8 and 16.7, respectively. However, owing to the large air damping, the frequency response in the low-vacuum chamber was barely detectable. The quality factors (air damping) of the resonators further indicate that the proposed approach could modulate the pressure of the sealed chambers. To calibrate the characteristics of quality factor versus ambient pressure, the resonators were also tested in a vacuum chamber. The results in figure 10(b) represent the quality factors measured at various chamber pressures. On the basis of the correlation between the results in figures 10(a) and (b), the air pressure in a high-vacuum sealed chamber ( $Q = 104.8$ ) was determined to be 1.3–1.4 mbar. The results agree reasonably with the pressure determined from the Pirani gauge.

#### 4. Conclusions

This study demonstrated the fabrication and integration of sealed micro-machined chambers with various vacuum conditions. Thus, the monolithic integration of sensors with various vacuum requirements, such as resonators, accelerometers, and gyroscopes, can be achieved. By varying the number and size of the embedded cavities, the vacuum conditions of the sealed chambers can be modulated. In addition, the cavities embedded in the substrate under various devices could be connected across the bonding ring by using an underground tunnel. Thus, the cavity arrangement as well as the modulation of vacuum conditions is flexible. In summary, this study presents a technique for achieving a wide range of vacuum conditions in sealed chambers to meet the requirements for various applications. To demonstrate the feasibility of the proposed process scheme, resonators and Pirani gauges were fabricated and characterized. The vacuum condition of the sealed chambers was then monitored using the quality factor of resonators and the pressure measured by Pirani gauges. The sealed chambers with vacuum conditions ranging from approximately 2 to 180 mbar were simultaneously fabricated and integrated on the same wafer. Moreover, the quality factor of resonators in the sealed chambers varied from approximately 0 (the dynamic response was suppressed by air damping and was scarcely measured) to  $Q = 104.8$ . The

approach demonstrated in this study can be combined with the technology presented in [22] to further increase the volume variation of sealed chambers. Thus, a wider vacuum condition of sealed chambers for wafer-level bonding can be implemented.

#### Acknowledgments

The authors wish to thank NTHU Micro Device Laboratory and Taiwan Semiconductor Manufacturing Company, Ltd for providing the sensor-related manufacturing and testing facilities.

#### References

- [1] Cheng C-W et al 2012 Bulk-Si with poly bump process scheme for MEMS sensors *Proc. IEEE Sensors Conf. 2012 (Taipei, Taiwan, October 2012)* pp 1–4
- [2] Castoldi L 2012 The MEMS revolution *SEMICON Italy (Milano, Italy, September 2012)*
- [3] Beer L 2014 The MEMS sensor integration path *SEMICON China (Shanghai, China, March 2014)*
- [4] Liu C-M et al 2011 MEMS technology development and manufacturing in a CMOS foundry *Transducers 2011 (Beijing, China, June 2011)* pp 801–805
- [5] Renard S 2000 Industrial MEMS on SOI *J. Micromech. Microeng.* **10** 245–249
- [6] Sun C-M et al 2009 Monolithic integration of capacitive sensors using a double-side CMOS MEMS post process *J. Micromech. Microeng.* **19** 015023
- [7] Fang W et al 2013 CMOS MEMS: a key technology towards the 'more than Moore' era *Transducers 2013 (Barcelona, Spain, 16–20 June 2013)* pp 2513–8
- [8] Robert P 2014 MEMS at Leti: new trends *SEMICON West (San Francisco, USA, July 2014)*
- [9] Guo B et al 2011 Above-IC generic poly-SiGe thin film wafer level packaging and MEM device technology: application to accelerometers *IEEE MEMS 2011 (Cancun, Mexico, 23–27 January 2011)* pp 352–5
- [10] Wang B et al 2011 Outgassing study of thin films used for poly-SiGe based vacuum packaging of MEMS *Microelectron. Reliab.* **51** 1878–81
- [11] Villarroya M et al 2006 A platform for monolithic CMOS-MEMS integration on SOI wafers *J. Micromech. Microeng.* **16** 2203–10
- [12] Takao H et al 2010 A versatile integration technology of SOI-MEMS/CMOS devices using microbridge interconnection structures *IEEE J. Microelectromech. Syst.* **19** 919–26
- [13] Fischer A C et al 2015 Integrating MEMS and ICs *Microsyst. Nanoeng.* **1** 1–16
- [14] Cheng C-W et al 2013 Single chip process for sensors implementation, integration, and condition monitoring *Transducers 2013 (Barcelona, Spain, 16–20 June 2013)* pp 730–3
- [15] Houlihan R et al 2005 Modelling squeeze film effects in a MEMS accelerometer with a levitated proof mass *J. Micromech. Microeng.* **15** 893–902
- [16] Liu K et al 2009 The development of micro-gyroscope technology *J. Micromech. Microeng.* **19** 113001
- [17] Li Q et al 2009 Outgassing of materials used for thin film vacuum packages *Int. Conf. on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP) (Beijing, China, August 2009)* pp 802–6
- [18] Lee B et al 2003 A study on wafer level vacuum packaging for MEMS devices *J. Micromech. Microeng.* **13** 663–9

- [19] Cheng S W *et al* 2015 Modulate the chamber pressure of the hermetic sealed MEMS device by varying the cavity depth of cap Si *IEEE Sensors Conf. 2015 (Busan, South Korea, November 2015)* pp 978–81
- [20] Liang K-C *et al* 2013 Wafer level packaging for chamber of two pressures *Transducers 2013 (Barcelona, Spain, 16–20 June 2013)* pp 1075–8
- [21] Shaw K A *et al* 1994 SCREAM I: a single mask, single-crystal silicon, reactive ion etching process for micro-electromechanical structures *Sensors Actuators A* **A40** 63–70
- [22] Liang K-C *et al* 2012 A novel low pressure sensor with fin-structures *IEEE Sensors Conf. 2012 (Taipei, Taiwan, October 2012)* pp 672–5