

Microdevice array design and fabrication in monolithic MEMS SoC

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This Letter presents a simple approach to fabricate the monolithic MEMS system on chip by means of adopting the 0.35 μm bipolar-CMOS-DMOS process with a single 3 μm -thick metal structure layer. The performance specifications are simply defined by the geometries of the metal proof-mass and the spring in these designs. The proposed designs include the out-of-plane and in-plane mechanical structures in different matrix arrays. No stress-induced deformation was observed in each single device within wide operation ranges of temperature. Simulation data of frequency responses at 14.22 and 2.71 kHz fit well with the measurement ones in each design. This potentially provides a novel advantage for the scalability to further integrate flattened microstructures with on-chip functional circuits for enhancing the system performance. The authors successfully demonstrate a platform for simplifying the designs that are applicable for inertial sensors, optical mirrors and biodetectors.

1. Introduction: Conventional CMOS processes have been extensively exploited to fabricate MEMS devices. The monolithic component integration of CMOS and MEMS in a single chip can then be achieved and many possible applications such as inertial sensor, biomedical system and/or their combinations integrated for fusing more consumer and industrial functionalities are revealed [1]. CMOS–MEMS technology offers the advantages of signal enhancement, electrical conducting compatibility and zero-level packaging [2]. Nevertheless, traditional designs are limited to the composite film stacking in back-end CMOS processes to build the mechanical structures and their performance would therefore be down-graded.

The implementation of CMOS-based inertial sensor using standard foundry processes has been extensively investigated [3]. For instance, CMOS inertial sensor has the advantage of monolithic integration of MEMS and integrated circuit (IC) and fully differential sensing can be easily implemented by electrical metal routing. To overcome the design limitation in the standard CMOS processes, various methods have been reported [4–8]. However, the deep reactive ion etcher and complicated additional processes are required [5–7], and the control of the proof-mass therefore becomes a critical concern. The main effort on stress compensation can be achieved by heating technique [7], yet it still faces the unpreventable temperature-coefficient-mismatch-induced structure curling [8].

Since double diffused MOS (DMOS) is proven to provide highly linear driving capability, the advanced bipolar-CMOS-DMOS (BCD) we used potentially fulfils the advantages of high sensing sensitivity, compact processing circuits, together with electrostatic actuation functions. In this Letter, we adopt the 0.35 μm BCD 4-metal technology [9] with a final post-oxide-etching process to achieve flexible device designs such as thumbtack-like structure arrays. Taking advantage of the multi-electrodes underneath, we obtain differential capacitances to sense the movement amplitudes and directions. This provides a new approach for tunable inertial sensor or biomedical devices, which are non-achievable by conventional types of the comb-drive multi-axis accelerometers [10, 11] or other bioMEMS [12]. In-plane rotation structure with lateral sensing stators is also obtained. These kinds of designs reveal potential for using a straight-forward and stable process to build the platform on various MEMS applications and further fulfil the higher performance system level integration chips.

2. Micro devices design: Fig. 1 illustrates the proposed design concept for the MEMS devices based on the advanced 0.35 μm

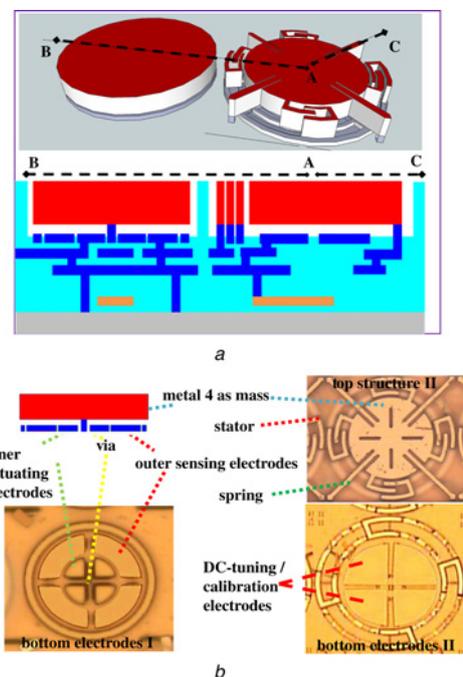


Figure 1 Design concept of the proposed microdevices
a 3D and cross-section views of the structures
b Descriptions of the proposed design in detail

BCD 4-metal technology with 3 μm -thick top aluminium layer. Shown in Fig. 1a, the three-dimensional and the cross-sectional views of the out-of-plane and in-plane microstructures both consist of the proof-masses, springs and electrodes. This structure implies that without affecting the functional ICs underneath, simply by adopting two of the upper layers in standard semiconductor processes, we can fabricate devices such as accelerometers or gyroscopes easily by designing their single-mass-layer geometries with sensing pad layouts. Fig. 1b describes examples of the device design considerations. For the thumbtack-like structure in the upper-left part of Fig. 1a, we use metal-4 layer as the proof-mass, the via between metal-4 and metal-3 to act as the spring and exploit metal-3 layer for capacitive sensing and electro-static actuating electrodes, mechanical vibration stopper ring and electrical interconnects to the on-chip circuits right underneath or in neighbourhood areas. Lower-left photo in Fig. 1b shows the

Table 1 Key design parameters of the device structures in MEMS system on chip (SoC)

Key design parameters	Structure code		
	$\times 10$	$\times 20$	$\times 30$
Proof mass geometry (μm)	$\Phi = 25, t = 3$	$\Phi = 50, t = 3$	$\Phi = 50, t = 3$
Spring geometry (μm)	W/L = 0.4/0.4, H = 0.9	W/L = 1/45, N = 4	W/L = 1/25, N = 2
Effective electrode area ratio	42% (sen.)/14% (act.)	62% (DC-tune)	62% (DC-tune)
Array matrix (row/column)	15/25	4/6	4/6
Potential applications	inertial sensor, resonator, mirror array, biomedical device	gyroscopes, mirror array	gyroscopes

layout of the multi-electrodes underneath the thick structures. Outer quadrant electrodes can sense the differential capacitance changes. In the case of the gyro-like structure in the upper-right part of Fig. 1a, the springs can be made by the same layer of the thick proof-mass diagonally stretched, with the via acting as the post for anchors. The sensing mechanism can be achieved by the same-layer rotor and stator pairs in capacitance change as exhibited in Fig. 1b. For precise detection and frequency matching, bottom electrodes here help to fine tune biases or for calibration. Optional layout of slots inside the top structures (displayed in the upper-right photo in Fig. 1b) cannot only be used for speeding up the post-micromachining process, but can also be designed to act as the damping ratio tuning while the device vibrates.

Table 1 lists three examples to show the key design parameters in the devices proposed. The thickness of the top aluminium layer is fixed at $3\ \mu\text{m}$ in the BCD technology we adopted. We can have various design numbers for different targeted structures. In the thumbtack-like device of $\times 10$, the diameter is set at $25\ \mu\text{m}$ for the proof-mass, the smallest spring we can obtain in this process is $0.4\ \text{by}\ 0.4\ \mu\text{m}$ with $0.9\ \mu\text{m}$ height. For its sensing electrodes, the quadrant-type design makes it possible for multi-degree-of-freedom detections by calculating or integrating the capacitances induced in the way of a fully differential sensing technique. We also add quadrant actuation pads close to the centre post that actively drive the top plate when positioning is a necessity. The ratio of the effective sense and actuation electrode areas compared with the full proof-mass is 42–14%; this makes more sensing efficiency than driving. The geometry of $\times 20$ is $50\ \mu\text{m}$ with four diagonal-symmetry-springs in a length of $45\ \mu\text{m}$. Compared with the array of 15 by 25 in $\times 10$ device, $\times 20$ has its matrix in 4 by 6. Another gyro-like 4 by 6 array device is $\times 30$, where two bridges are connected to the outer square ring by two $25\ \mu\text{m}$ beams. Although six stator-rotor pairs are sensing the in-plane rotation movement, the two-side-electrodes under the square ring are being used for DC-tuning or zero-state balancing.

A matrix can be flexibly designed; in some circumstances, several rows or columns might be able to act as dummy or redundant pixels for system level considerations. Choosing possible arrays arrangement and combination with different single device (or pixel) structures, we can therefore gain a great advantage on the specification scalability in MEMS performances. Take X10-series structure type, for example, where we can have the fundamental frequency responses designed from 1 kHz to 1.2 MHz; and in X20-series, the first mode lies between 1 and 200 kHz (at pixel pitches of $45\ \text{by}\ 45\ \mu\text{m}$ or $77\ \text{by}\ 51\ \mu\text{m}$). Figs. 2a and b reveal two mode shape results by ANSYS simulation of frequency responses of single $\times 10$ and $\times 30$ device, respectively. Besides, when they are matrix arrayed, the sensed signal will increase in scale; thus, we can obtain the predictable sensitivity improvements. Alternatively, with addressing technique, we can have selectively programmable manipulation for pixel-by-pixel sensing and control. In addition, the small die area (about 1 by 1 mm^2 or less) makes the phase differences or propagation delays of each pixel among a large number of array matrices unnoticeable. Therefore

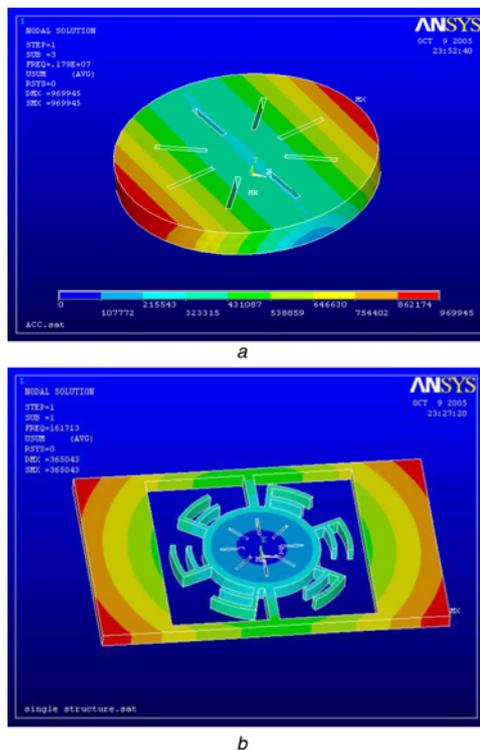


Figure 2 Two examples of the simulated frequency responses to observe the mode shapes of the designed devices
a $\times 10$ device
b $\times 30$ device

with this novel design we can gain flexibility in deploying the system performance.

3. Monolithic fabrication: The original foundry fab-out dice are monolithically integrating MEMS devices and circuit parts. To release the free-moving structures on the chips, we have to prevent the circuit area from undergoing the post-etching process to maintain its functionality. Therefore we cover the circuit part with the passivation layer with the MEMS parts unpassivatedly exposed for simple one-step dip-and-etch directly in the HF-based solution. Buffered HF or the mixture solution of ammonium fluoride and acetic acid such as Silox® etchant is used for releasing the mechanical parts from the inter-metal dielectrics such as pure oxide, without any complex dry-etching or masks (isopropyl alcohol (IPA) treatment for anti-stiction is optional), as shown in Fig. 3a with the cross-section diagram and the SEM photo of a finished die. This confirms that the MEMS devices are being well released without attacking the circuitry area inside the monolithic SoC. Fig. 3b is the microscopy photo with see-through image of sensing and conditioning circuits under the passivated part of the die. In this Figure, the basic functional blocks include oscillation clock to provide a reference modulation frequency, bandgap reference for

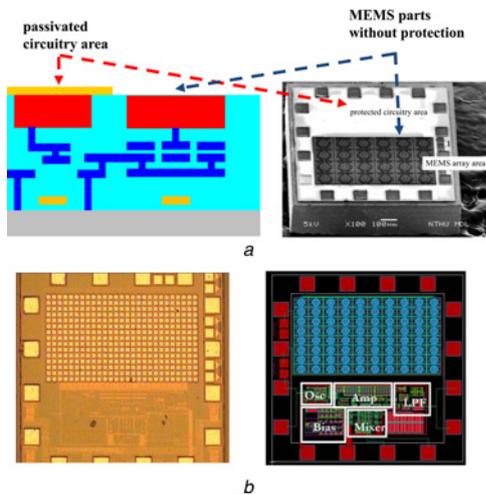


Figure 3 Monolithic fabrication
a Schematic and SEM photo show that the passivation can protect the circuitry area while the moving MEMS device being released
b Microscopic photo reveals the underlying integrated circuitry and refers to the identified functional blocks in layouts

biasing sources, low-noise amplifier to read out the capacitive signals, mixer to demodulate and multiply the carrier with mechanical vibration frequencies and then filter for passing high band signals, are identified in the right layout.

Thus, the foundry available process together with in-house post-micromachining offers a simple approach to fabricate the monolithic MEMS systems.

4. Results and discussion: In present mature semiconductor processes, tiny structured pixel-array gains the most benefit of the high yield rate (and hence also higher reliabilities). Nevertheless, strictly defined layout rules of dummy structures for uniformly etching process might result in few microrod residues that need to shake away carefully and gently during the post-etching process.

Fig. 4 presents the SEM photos of the three instances in our MEMS device structure design. Enlarged views and matrix array of $\times 10$, $\times 20$ and $\times 30$ are shown in Figs. 4*a–c*, respectively. Observed from Fig. 4*a*, we found that a 500 nm gap under the top circle plate of $3\ \mu\text{m}$ thickness provides the travel distance of $\times 10$'s out-of-plate vibration. The released matrix array shows clean and well-defined profiles without demonstrating any deformation. Besides, the out-stretched beams and the inter-digit rotor-stator pairs reveal any stiction issues in these structures.

Further investigation of the single metal layer structure of type $\times 10$ by optical interference technique of WYKO scan, proves the flat surfaces and profiles without detectable curvature in Fig. 5*a*. During elevation with the temperature increasing from 20 to 80°C by industrial standards, we cannot record any warpage profile or deformation happening to the devices. Fig. 5*b* draws the profiles in each temperature step of 10° . For the out-of-plane displacement measurement, we apply increased DC-bias voltages onto one of the four near-centre driving pads underneath its top mass. $\times 10$ behaves itself consistently with linear displacements below 40 V in this short travel range, after that, it will show non-reversible snap-down in attaching to the outer landing ring as shown in Fig. 5*c*. Although not in this case, driving voltages up to several tens of volts can be potentially actuated by the on-chip DMOS in the BCD technologies.

Frequency responses are also characterised with the laser Doppler velocimetry (LDV) and MEMS motion analysis (MMA) for obtaining the mode shapes of $\times 10$ and $\times 20$, respectively. One out-of-plane motion peak happens at 14.22 kHz (Figs. 6*a*) and 6*b* indicates that the in-plane fundamental motion sits on 2.71 kHz. Since the rigidity of the spring can be designed by its geometry,

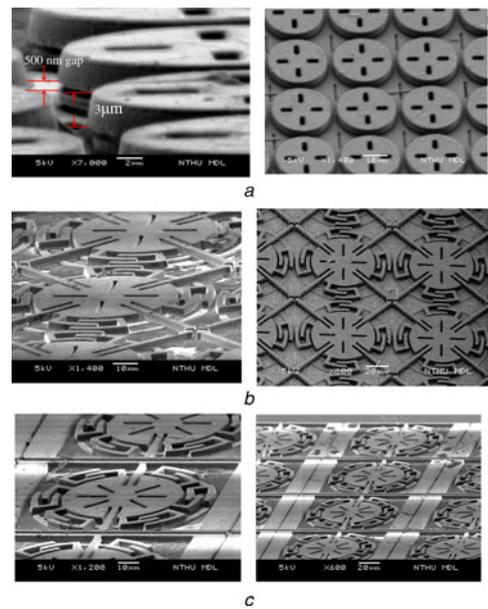


Figure 4 Enlarge views and matrix array by SEM photos in different type MEMS device designs

a $\times 10$
b $\times 20$
c $\times 30$

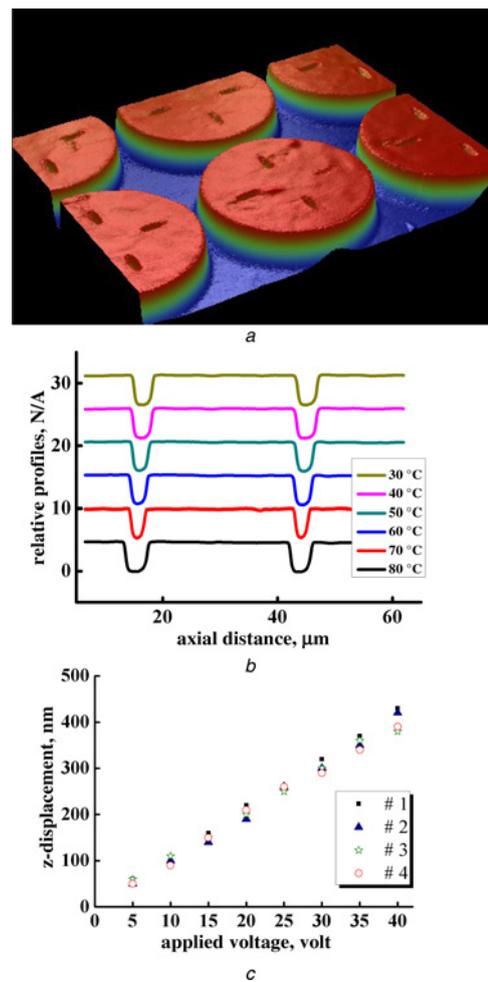


Figure 5 Characterisation of single metal layer structure of type $\times 10$
a WYKO scan reveals no warpage in single material mass of thick aluminium layer
b No deformation observed among wide temperature ranges
c Displacement of $\times 10$ against applied voltages

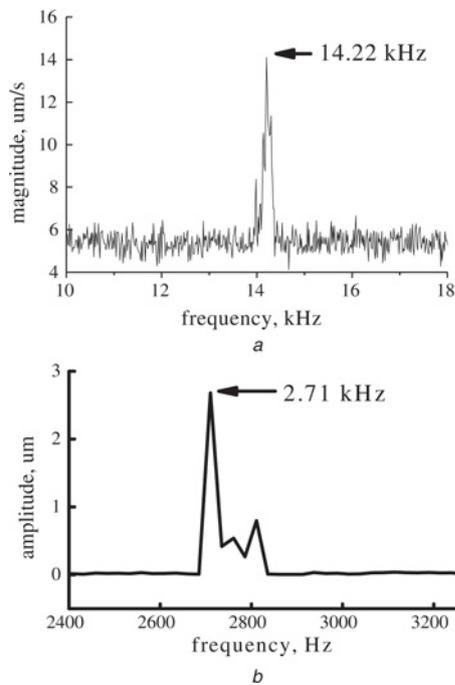


Figure 6 X10's out-of-plane motion by LDV spectra and X20's in-plane frequency response by MMA, respectively

considering that the symmetrical axial-length (i.e. aspect) ratio of $\times 10$'s mass and spring is as high as 62.5, it still has difficulty freely vibrating. Compared with the near-one aspect ratio of $\times 20$ structure type, the first mode in the frequency response falls at the range far below, implying the vibration of the springs is softer longitudinally than vertically. Nevertheless, again the frequency responses confirm that the flexibility in our designs can be achieved by simply adjusting the geometrical factors of the devices.

Multi-electrode designs in this study are divided into quadrant ones as the layouts shown in Fig. 1b; therefore the effective couplings might be degraded at least to 1/4 if we sense the signal by a single pad. Nevertheless, the array matrix can multiply the signals received, which again makes the signals suitable for featured applications such as inertial sensors. Respectively, addressing each device or triggering each divided electrode underneath the patterned structures with pixel-by-pixel signal process circuits can fulfil more intelligent manipulation in MEMS SoCs.

In addition to working on the electrical characterisations to confirm the applicability for some potential fields, we can further extend the structure layer to combine more metal layers and adopt one or several of the conduction layers for electrical driving and/or sensing. The low-cost glass frit technique is also taken into account in multi-chip packaging for the trend of sensor fusion. By combining scalable and tunable specification platform and high driving capability of the DMOS in this advanced BCD process, it is predicted that we can make both sensors and actuators perform more delicate interactions with simpler design strategies.

5. Conclusions: The study designs several different geometry structures by simply using the 3 μm top aluminium layer of the 0.35 μm BCD process. After one-step post-process etching, we release the moving parts to have out-of-plane and in-plane motions. The uniformity and flatness of the device surfaces come

directly from the well-controlled semiconductor fabrication and no temperature-induced material stress was observed by optical interference scans within the standard industrial temperature range. Part of the device electrodes can successfully drive the structure in displacements. Fundamental mode shapes are also measured, and turned out fitting the original simulated data around 14.22 and 2.71 kHz of the out-of-plane and in-plane frequency responses, respectively. This means that the simple design approach potentially competes with the conventional composite MEMS devices.

In this Letter, a single metal layer structure adopted from the standard semiconductor technologies proves no stress-induced deformations, which are applicable for various geometrical device designs in monolithic MEMS SoCs. Multi-electrodes layout further extends the detectable degree-of-freedom with sole proof-mass. Matrix-array arrangements also potentially fulfil the scalabilities in systematic performance specifications, which provide more flexible and predictable results. These two main advantages prove that we successfully leverage the simplest process to design the most promising platform for the microsystems.

6 References

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