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Post-CMOS selective electroplating technique for the improvement of CMOS-MEMS accelerometers

Yu-Chia Liu[1], Ming-Han Tsai[1], Tsung-Lin Tang[2] and Weileun Fang[1,2]

[1] Institute of NanoEngineering and MicroSystems, National Tsing Hua University, Hsinchu 30013, Taiwan
[2] Power Mechanical Engineering Department, National Tsing Hua University, Hsinchu 30013, Taiwan

E-mail: fang@pme.nthu.edu.tw

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Abstract
This study presents a simple approach to improve the performance of the CMOS-MEMS capacitive accelerometer by means of the post-CMOS metal electroplating process. The metal layer can be selectively electroplated on the MEMS structures at low temperature and the thickness of the metal layer can be easily adjusted by this process. Thus the performance of the capacitive accelerometer (i.e. sensitivity, noise floor and the minimum detectable signal) can be improved. In application, the proposed accelerometers have been implemented using (1) the standard CMOS 0.35 μm 2P4M process by CMOS foundry, (2) Ti/Au seed layers deposition/patterning by MEMS foundry and (3) in-house post-CMOS electroplating and releasing processes. Measurements indicate that the sensitivity is improved 2.85-fold, noise is decreased near 1.7-fold and the minimum detectable signal is improved from 1 to 0.2 G after nickel electroplating. Moreover, unwanted structure deformation due to the temperature variation is significantly suppressed by electroplated nickel.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Recently, complementary metal oxide semiconductor (CMOS) processes have been extensively exploited to fabricate microelectromechanical system (MEMS) devices. The monolithic integration of CMOS and MEMS components in a single chip can be achieved via this manner, and finds use in many applications such as RF-MEMS, biomedical, consumer and industrial electronics [1]. Such CMOS-MEMS technology provides the advantages of sensing signal enhancement, more electrical routing compatibility and zero-level packaging possibility [2]. However, the design of mechanical structures is limited to the standard thin-film stacking. Thus, the performances of CMOS-MEMS devices are then influenced. To enhance the design flexibility and improve the device performances, back-end processes to integrate materials other than the standard CMOS layers are investigated and demonstrated [3–8].

The CMOS-MEMS accelerometer implemented using the foundry available standard process has been extensively investigated [9]. The CMOS-MEMS accelerometer has the advantage of the monolithic integration of the MEMS and IC, and fully differential sensing is easily implemented using metal layers electrical routing. To overcome the design limitation due to the standard CMOS process, various methods for the sensitivity improvement of CMOS-MEMS accelerometers have been reported [10–14]. However, relatively complicated processes are required for [11, 12], and the control of the proof-mass thickness is also a critical concern. The stress compensation can be achieved by the heating technique to improve sensitivity [13], yet more power consumption is required for such a device. The design trade-off between the sensing electrode and proof mass will lead to the Brownian noise [14].

This study exploits the selective electroplating technique [15] to increase the mass and stiffness of the structures for the CMOS-MEMS accelerometer. Thus, the performance of

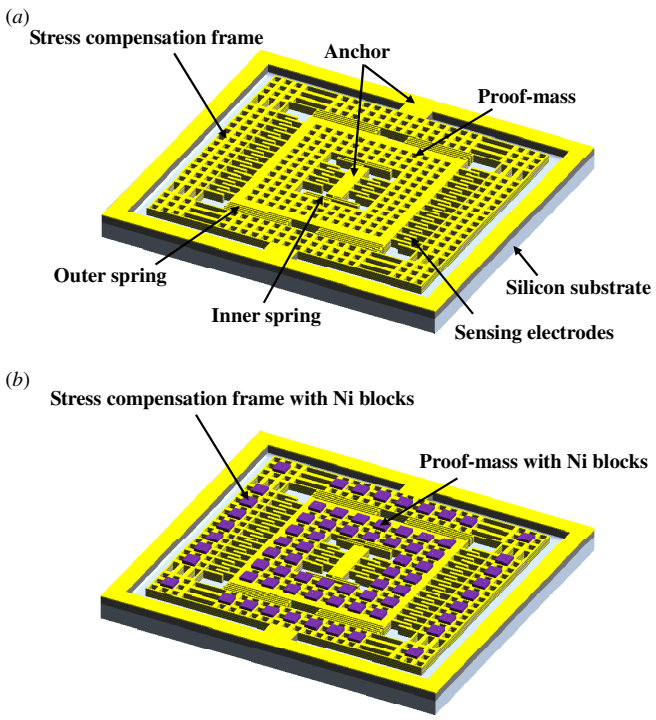


Figure 1. Design concept of the proposed accelerometer: (*a*) the existing design (without Ni) and (*b*) the proposed design (with selectively electroplated Ni blocks).

the CMOS-MEMS accelerometer can be improved by means of a simple post-CMOS process. The selective patterned metal seed layers (Ti/Au) are prepared by the MEMS foundry (*apm*, Asia Pacific Microsystems Inc., Taiwan) right after the standard CMOS process provided by the CMOS foundry (TSMC, Taiwan Semiconductor Manufacturing Company, Taiwan). Finally, metal electroplating is fabricated in-house without any photolithography process. In application, the accelerometer reported in [14] is fabricated using the 0.35 μm TSMC 2-polysilicon 4-metal CMOS process and then electroplated with Ni. The influence of electroplated Ni on the performances (such as sensitivity, noise, etc) of the CMOS-MEMS capacitive accelerometer is also investigated.

2. Sensor design and analysis

2.1. Sensor design

Figure 1 illustrates the proposed design concept to improve the CMOS-MEMS sensor. Figure 1(*a*) shows the existing hollow proof-mass CMOS-MEMS accelerometer consisting of the proof mass, sensing electrodes, outer and inner springs and stress compensation frame [14]. The accelerometer has an equivalent proof mass M and spring stiffness K, and the initial sensing gap between the stationary and moving comb-finger electrodes is g_o. For an open-loop sensing mechanism, the capacitive accelerometer, with a measured acceleration of A_{cc} and an output voltage of V_{out}, has a sensitivity of [16],

$$S_{acc} = \frac{\Delta V_{out}}{A_{cc}} = S_{mech} \times G_{amp} \tag{1}$$

$$S_{mech} = \frac{M}{K} \times \frac{C_o}{g_o} \times \frac{4V_m}{(C_p + 2C_o)}, \tag{2}$$

where C_o is the initial capacitance for the all-sensing electrode, C_p is the parasitic capacitance, V_m is the input modulation voltage and G_{amp} is the circuit gain. According to equations (1) and (2), a larger proof mass will improve the sensitivity of the micro-accelerometer. Moreover, the Brownian noise equivalent acceleration (BNEA) can be expressed as [17]

$$\text{BNEA} = \frac{\sqrt{4k_B T b}}{9.8M}, \tag{3}$$

where k_B is the Boltzmann constant, T is the absolute temperature and b is the damping coefficient. As indicated in equation (3), a larger proof mass will provide a better BNEA performance and thus improve the minimum detection signal (MDS) of the micro-accelerometer. However, as limited to the thickness of stacking films, the CMOS-MEMS accelerometer has a relatively small proof mass. As shown in figure 1(*b*), this study presents the concept to selectively electroplate nickel blocks on top of the CMOS chip to improve the performance of the CMOS-MEMS accelerometer. Thus, the proof mass M of the CMOS-MEMS accelerometer can be increased to improve its sensitivity and MDS. In addition, the bending stiffness of the CMOS-MEMS structures can also be modulated by varying the pattern and thickness of Ni blocks. Hence, the bending deformation of the CMOS-MEMS structures induced by the coefficient of thermal expansion (CTE) mismatch of thin films can be reduced.

The presented approach to improve the performance of the CMOS-MEMS accelerometer using selective electroplated Ni has the following advantages: (1) selective electroplating of the nickel blocks can be easily achieved using the patterned metal seed layers on the top of the CMOS chip, (2) the thickness of Ni can be easily adjusted by post-CMOS electroplating processing to change the mass and stiffness of the MEMS structures, (3) post-CMOS electroplating is a room temperature process and will not affect the CMOS circuits formed by metal layers and (4) the Ni film has large density and elastic modulus to effectively improve the mass and stiffness of the MEMS structures.

2.2. Sensor analysis

This study employs the design listed in table 1 to predict the typical characteristics of the presented accelerometer. The design of the structure is based on the standard TSMC 0.35 μm 2P4M CMOS process, and thus the maximum thickness of the CMOS-MEMS structure is 6.97 μm. The thickness of the Ni layer defined by the in-house post-CMOS electroplating is 4 μm. Other important planar dimensions of MEMS structures defined by the photolithography and etching processes are also depicted in the design layout in figure 2. The planar patterns defined for Ni electroplating are designed as 22 μm $\times$ 22 μm, and there are 76 Ni blocks in total defined on the proof mass. The discrete Ni blocks instead of the continuous Ni layer are designed to reduce the bending deformation of the suspended MEMS structures caused by the

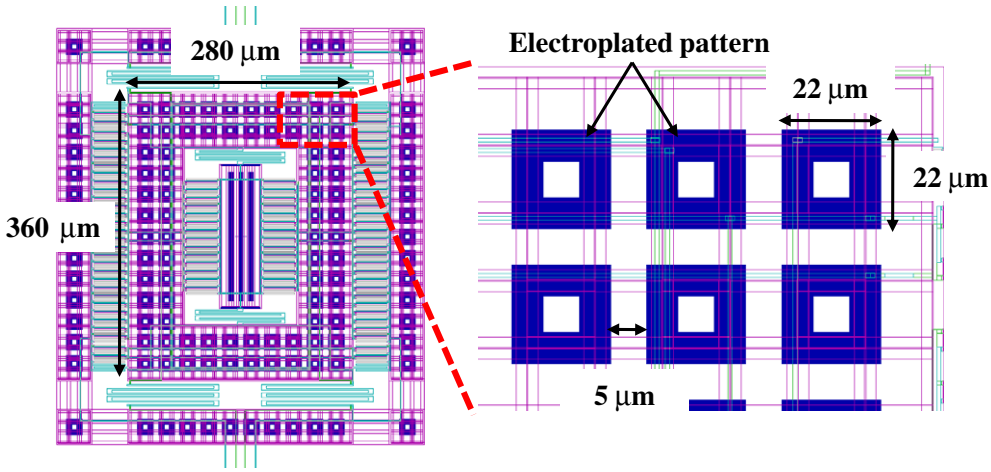


Figure 2. The design layout to show the planar dimensions of the electroplated patterns on the proof mass and stress compensation frame.

Table 1. The design parameters and specifications of the proposed CMOS-MEMS accelerometers with and without electroplated Ni.

Major dimensions of the sensing element		
Proof-mass size	$280 \times 360\ \mu m^2$	
Comb finger gap (g_o)	$1.5\ \mu m$	
CMOS layer thickness	$6.97\ \mu m$	
Electroplated pattern size	$22 \times 22\ \mu m^2$	
Electroplated Ni thickness	$4\ \mu m$	
Length of the sensing electrode	$55\ \mu m$	
Width of the sensing electrode	$4.2\ \mu m$	
Design specifications of the sensing element		
	Without Ni	With Ni
Inner spring stiffness (K_{in})	1.92 N m^{-1}	1.92 N m^{-1}
Outer spring stiffness (K_{out})	1.32 N m^{-1}	1.32 N m^{-1}
Resonance frequency	6.94 kHz	4.3 kHz
Weight of proof mass (M)	1.01 μg	2.63 μg
Initial sensing capacitance (C_o)	96 fF	96 fF
Mechanical sensitivity (S_{mech})	0.19 mV G^{-1}	0.51 mV G^{-1}
Sensitivity ($G_{amp} = 23$ dB)	2.68 mV G^{-1}	7.2 mV G^{-1}
BNEA	227.1 μG Hz$^{-1/2}$	87.2 μG Hz$^{-1/2}$
TNEA	332 μG Hz$^{-1/2}$	125.5 μG Hz$^{-1/2}$

residual stress of the Ni film. The mechanical properties and electrical output of the accelerometer are then predicted by commercial finite element software (ConventorWare). The simulation results show that the accelerometers with and without Ni blocks have the same stiffness for inner and outer springs, whereas the resonant frequency of the accelerometer drops from 6.94 to 4.3 KHz after adding the electroplated Ni blocks. As a result, the proof masses of the accelerometer are respectively 1.01 μg (without Ni) and 2.63 μg (with Ni). Thus, the electroplated nickel blocks significantly increase the mass of the CMOS-MEMS accelerometers.

In this study, the initial sensing capacitance determined from the dimensions and gap of sensing electrodes is $C_o = 96$ fF. Moreover, based on the design of electrical routings, the parasitic capacitance of the accelerometers is estimated as $C_p = 500$ fF. According to equation (2), as the accelerometers are having an input modulation voltage of $V_m = 1$ V, the corresponding mechanical sensitivities S_{mech} are calculated as 0.19 mV G^{-1} (without Ni) and 0.51 mV G^{-1} (with Ni). According to equation (3), the BNEA is decreased from 227.1 to 87.2 μG Hz$^{-1/2}$ after adding electroplated Ni blocks. Thus, the MDS can be further enhanced. The fully differential readout circuit schematic as shown in figure 3(a) is improved from the design of [18]. The common mode feedback circuit schematic provides a more robust dc level during the measurement. Figure 3(b) shows the continuous time, fully differential sensing architecture employed in this study. The cross-axis sensitivity and noise performance can be minimized under this condition [19]. The total noise equivalent acceleration (TNEA) can be determined from [17]

$$\mathrm{TNEA} = \sqrt{\mathrm{BNEA}^2 + \frac{v_n^2}{S_{mech}^2}}, \tag{4}$$

where v_n is the input-referred circuit noise. Since the noise floor of the readout circuit predicted from commercial software

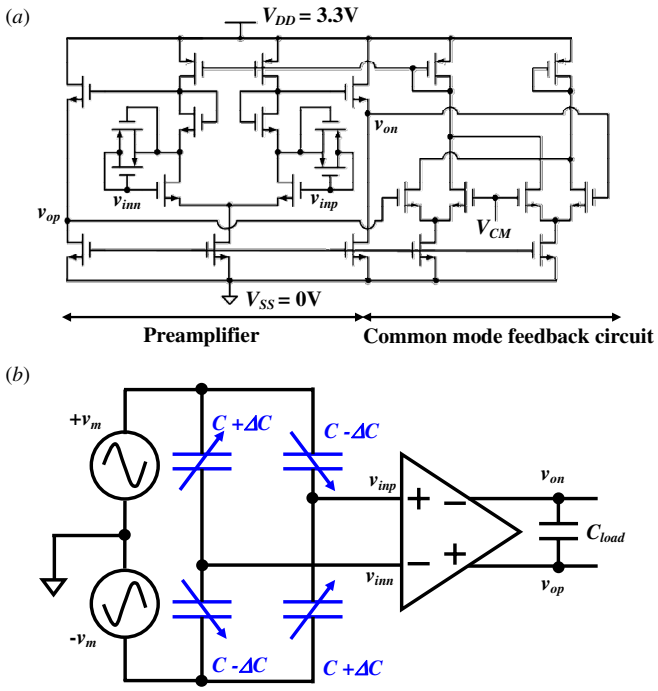


Figure 3. (*a*) Schematic of a fully differential readout circuit and (*b*) architecture of a fully differential sensing design.

(HSPICE) is 46 nV $Hz^{-1/2}$, the TNEAs determined from equation (4) are respectively 332 μG $Hz^{-1/2}$ (without Ni) and 125.5 μG $Hz^{-1/2}$ (with Ni).

3. Post-CMOS fabrication and results

Figure 4 illustrates the process steps. As shown in figure 4(*a*), the thin-film stacking and patterning were prepared by foundries [20]. The CMOS layers were prepared by the CMOS foundry TSMC, and the deposition and patterning of Ti/Au seed layers were fabricated by the MEMS foundry *apm*. The minimum line width and spacing of Ti/Au layers are 5 μm. Since the patterns of MEMS structures and Ni blocks were defined by the foundries, thus no masks and photolithography processes were required for the post-CMOS fabrication. Figures 4(*b*)–(*d*) show the in-house electroplating and post-release processes. As indicated in figure 4(*b*), the CMOS-MEMS chip was wire bonded after adhered to a handling wafer with Ti/Au layers. After that, the CMOS-MEMS chip and its handling wafer were immersed into the plating solution during the electroplating process. The dielectric SiO_2 layer was exploited as the electrical isolation, and only electroplating pads and Ti/Au layers were exposed to the plating solution. As indicated in figure 4(*c*), after applying the dc current to the chip through the handling wafer and on-chip electrical routings, the nickel blocks were selectively electroplated on top of the Ti/Au layer. The thickness and residual stresses of the electroplated nickel were controlled by the plating conditions, such as the applied current density and the plating time. Thus, the nickel material is successfully electroplated on the proof mass and stress compensation frame. However, there was no mold structure (such as photo-resist) to define the

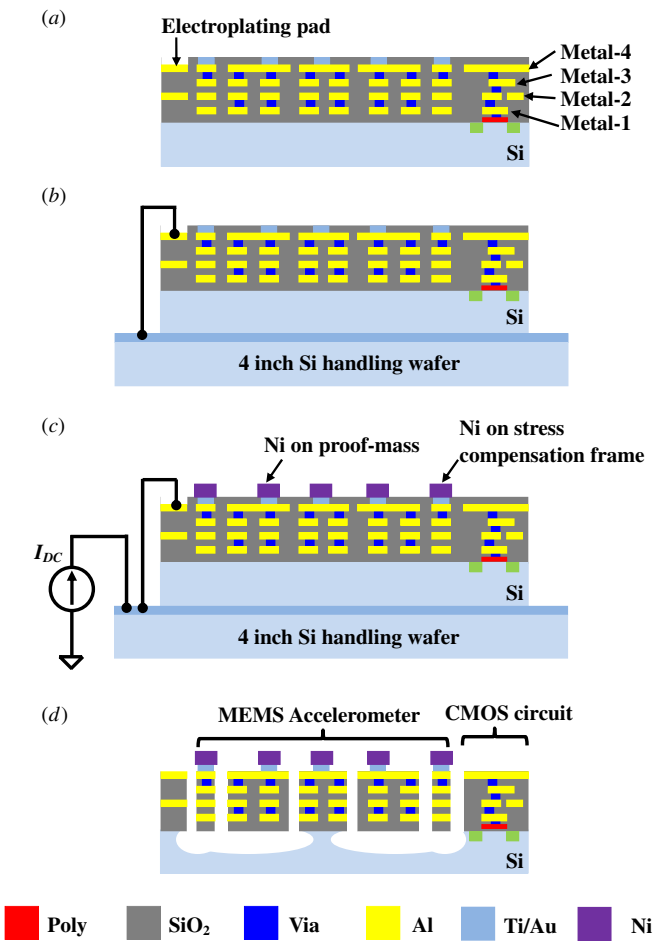


Figure 4. Fabrication process steps: (*a*) chip prepared by TSMC and *apm*, (*b*) wire bonding for dc current supply, (*c*) in-house post-CMOS Ni electroplating and (*d*) RIE and XeF_2 for structure releasing.

electroplating area, and the plating time needed to be properly controlled to prevent the etching release holes being totally covered by nickel. In this study, the thickness of electroplated Ni was 4 μm under the conditions of 25 min plating time and 2 mA dc current. Such electroplating condition can lower the residual stress of the Ni layer. Moreover, the stiffness of the MEMS structure is increased by the additional Ni layer, so that the bending deformation by the residual stress of the Ni film can be suppressed. As shown in figure 4(*d*), the structure was then defined by reactive ion etching (RIE) and finally suspended after the Si substrate was isotropically etched by XeF_2. The metal-4 acted as the hard mask during the post-CMOS process.

The scanning electron microscopy (SEM) micrograph in figure 5(*a*) shows the typical fabricated chip consisting of the accelerometers with and without electroplated Ni. Note that the readout circuit not being observed in the SEM micrograph is also inside the chip. The zoom-in micrographs in figures 5(*b*) and (*c*) show that the Ni blocks are uniformly and selectively electroplated onto the proof mass and stress compensation frame of the released CMOS-MEMS accelerometer. The sensing electrodes and Ni block can be further clearly observed in the zoom-in micrograph of figure 5(*d*). Thus, the foundry

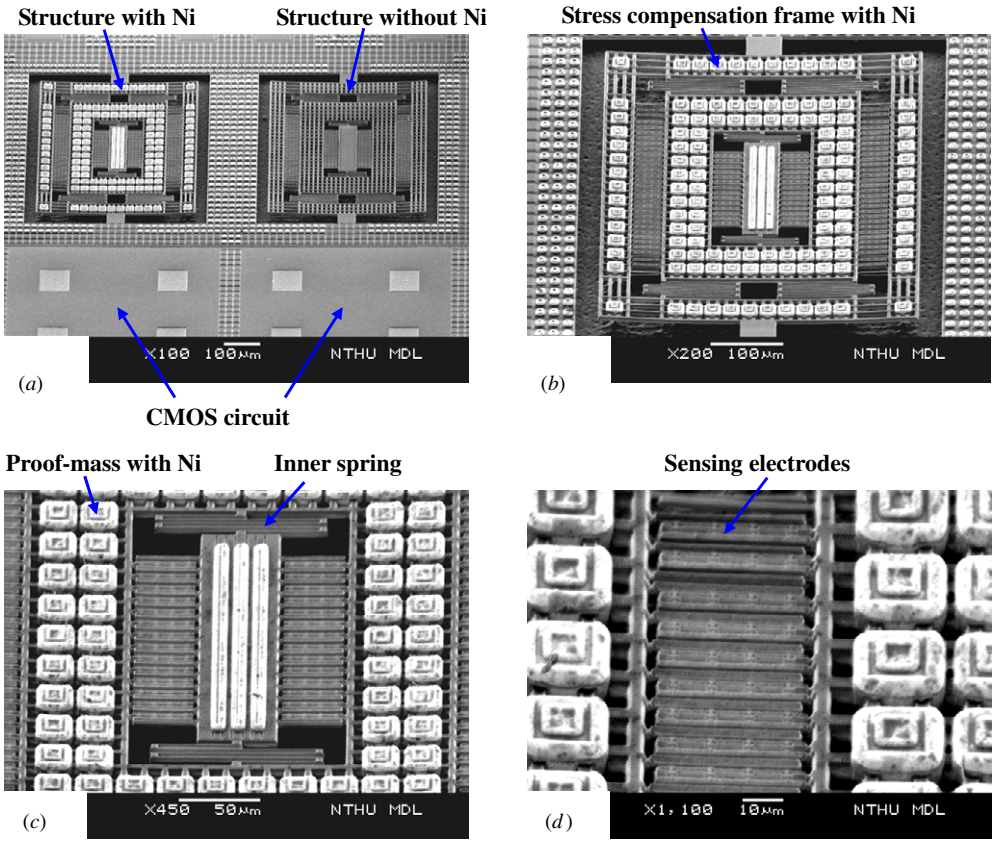


Figure 5. SEM micrographs of (*a*) the monolithic integration of the MEMS and IC, (*b*) the accelerometer with electroplated Ni, (*c*) zoom-in view of selectively electroplated Ni and (*d*) zoom-in view of Ni blocks.

available processes together with the in-house post-CMOS process provide a simple approach to fabricate the CMOS-MEMS accelerometer. The measurement from an optical interferometer in figure 6(*a*) shows the surface profile of the accelerometer before releasing from the substrate. The measurement in figure 6(*b*) shows the surface profile along the AA′ cross section indicated in figure 6(*a*), and the thickness of electroplated nickel is 4.01 ± 0.22 μm with five different samples.

4. Experimental results and discussion

The chip is packaged in ceramic housing as shown in figure 7(*a*) for mechanical and electrical tests. Figure 7(*b*) shows the frequency response characterized by the commercial optical stroboscope system. The results indicate that the resonant frequency of the structure is decreased 1.76-fold after adding the proof mass by electroplated nickel. The measured natural frequencies for both accelerometers are higher than the simulation ones, and the deviations are approximately 13.3% (without Ni) and 3.72% (with Ni), respectively. The deviations are mainly due to the geometric variation of springs, and Ni blocks resulted from the post-CMOS fabrication processes.

The accelerometer was tested by the setup shown in figure 8(*a*). The input acceleration is specified by the commercial shaker (LDS Inc., V406) and calibrated by a

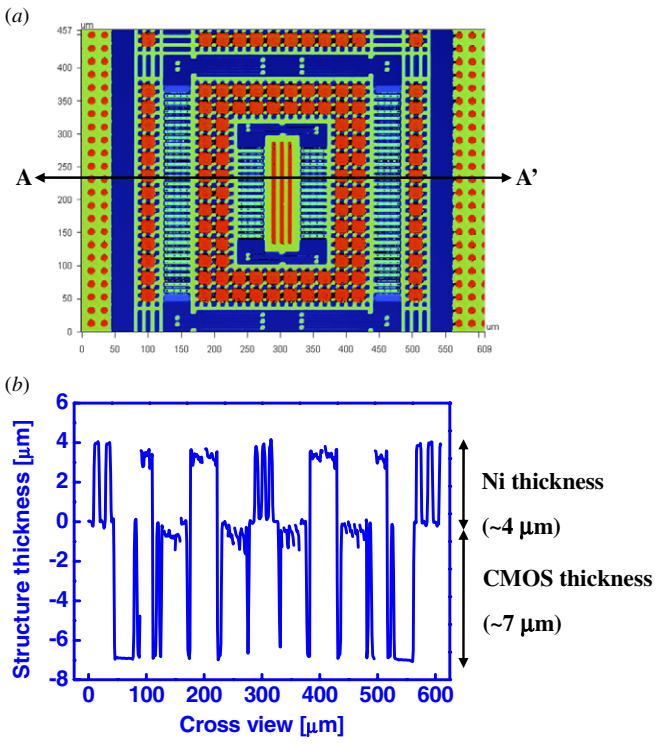


Figure 6. Measured (*a*) surface profile and (*b*) corresponding Ni blocks before structure releasing.

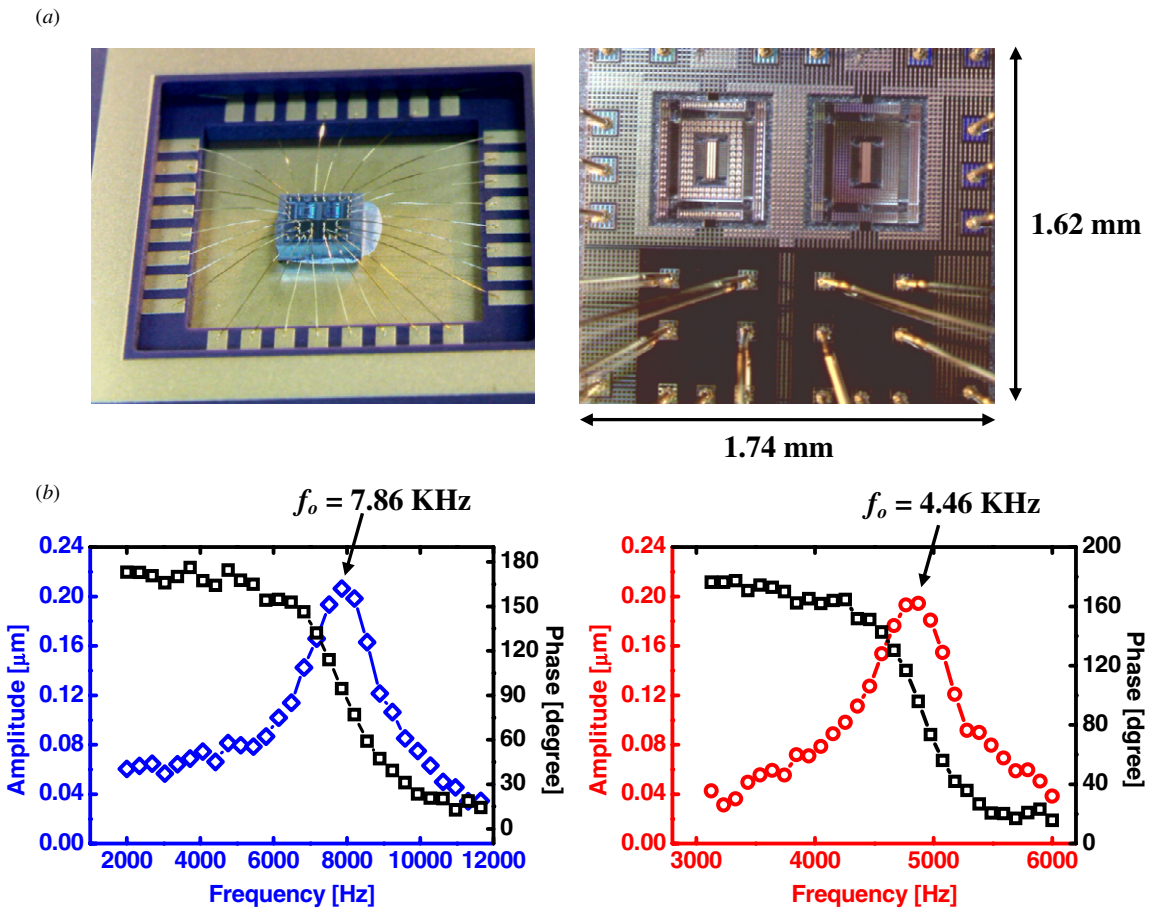
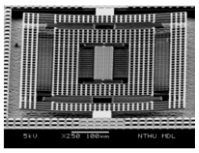
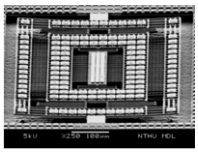


Figure 7. (*a*) Accelerometer packaged in a ceramic housing and (*b*) measured frequency responses for accelerometers with and without Ni.

commercial piezo-based accelerometer (PCB Piezotronics Inc., Model-352C44). The modulation signal is provided by the function generator (Tektronix Inc., AFG-3022). The measurement results in figure 8(*b*) show the output voltages of accelerometers at different accelerations. It indicates that the sensitivity S_{acc} of the accelerometer is increased from 1.47 to 4.19 mV G^{-1} (i.e. increased 2.85-fold) after Ni electroplating. Moreover, the measurements also show that the MDS of acceleration are further improved from 1 to 0.2 G after Ni electroplating because of the larger sensitivity. There are several possible reasons to cause the measured sensitivity to be smaller than the analytical one. First, the movable and fixed sensing electrodes are not perfectly overlapped due to the residual stresses. Second, the parasitic capacitance is induced by the metal-4 hard mask.

The measurement results displayed by the spectrum analyzer (Agilent Inc., 4395A) in figures 8(*c*) and (*d*), respectively, show the frequency responses of accelerometers with and without electroplated Ni. The accelerometers are under a vibration excitation of 1 G and 100 Hz, and have a modulation signal of 1 MHz and 1 V_{p-p}. The overall noise floor of −102.8 (corresponding to 7.23 μV_{rms} $Hz^{-1/2}$) and −98.2 dBV (corresponding to 12.28 μV_{rms} $Hz^{-1/2}$) indicated in figures 8(*c*) and (*d*) were measured respectively at 1 Hz resolution bandwidth. According to the measured sensitivity S_{acc} from figure 8(*b*) and equation (4), the TNEAs are determined from the overall noise floor as 6.94 mG $Hz^{-1/2}$ (without the Ni layer) to 4.13 mG $Hz^{-1/2}$ (with the Ni layer). Thus, the TNEA is decreased after the electroplating of the Ni layer. Table 2 summarizes the comparison of measurement results from the CMOS-MEMS accelerometers with and without electroplated Ni blocks. In short, the electroplated Ni block successfully improves the performances of the CMOS-MEMS accelerometer in terms of the sensitivity, noise floor and minimum detection signal.

Table 2. Measurement results to show the comparison of CMOS-MEMS accelerometers with and without electroplated Ni.

		
Frequency (kHz)	7.86	4.46
Sensitivity (mV G^{-1})	1.47	4.19
Nonlinearity (%)	2.38	2.11
X-cross-axis coupling (%)	2.36	2.28
Z-cross-axis coupling (%)	4.77	4.35
TNEA (mG $Hz^{-1/2}$)	6.94	4.13
MDS (G)	1	0.2

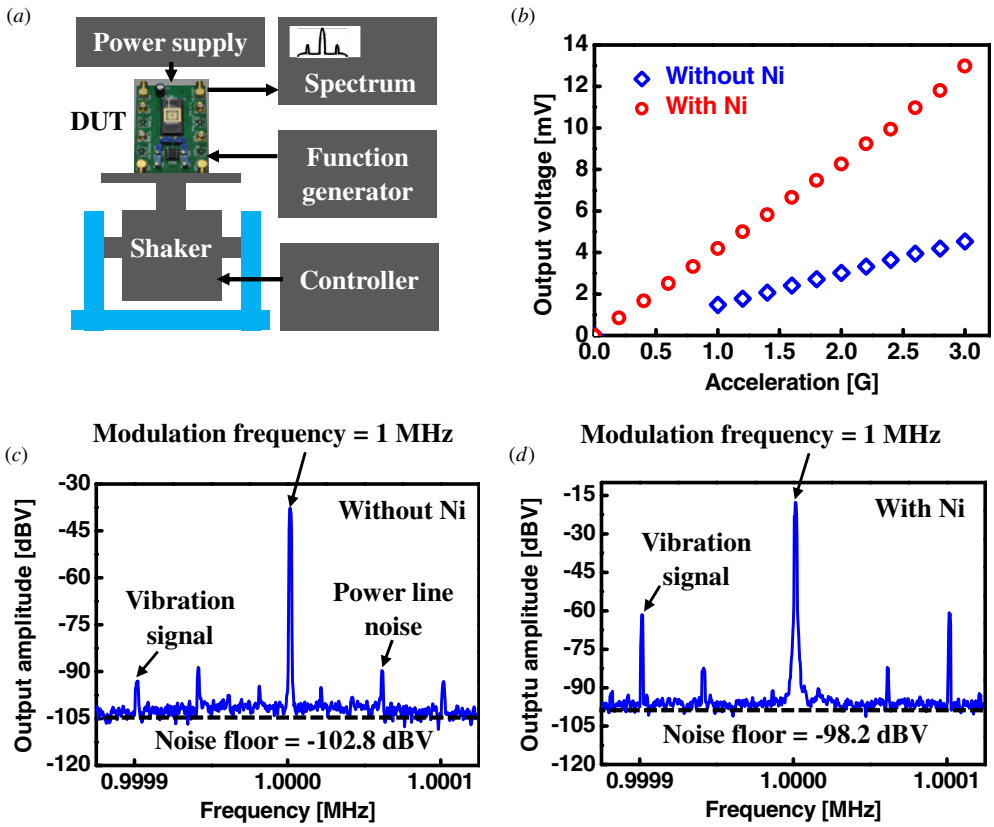


Figure 8. (*a*) Measurement setup for the accelerometer sensitivity test, (*b*) the measured output voltages versus input accelerations, and (*c*), (*d*) measurements of accelerometers from the spectrum analyzer under the excitation of 1 G at 100 Hz (resolution bandwidth = 1 Hz).

Table 3. Comparison of the presented and the existing single-axis CMOS-MEMS accelerometers.

	Xie *et al* [11]	Lakdawala *et al* [13]	Sun *et al* [14]	This study (with Ni)
Technology	HP 0.5 μm 1P3M	HP 0.5 μm 1P3M	TSMC 0.35 μm 2P4M	TSMC 0.35 μm 2P4M
Proof-mass dimension (μm)	–	200 × 200	440 × 490	280 × 360
Weight of proof mass (kg)	–	0.47×10^{-9}	0.85×10^{-9}	2.63×10^{-9}
Sensing gap (μm)	–	–	1.5	1.5
Sensing capacitance (fF)	–	193	112	96
Heater power consumption (mW)	No need	20–100	No need	No need
Fabrication level	Complicate (double-side DRIE)	Easy	Easy	Easy
Resonance frequency (kHz)	4.1	5.61	5.83	4.46
Sensitivity (mV G^{-1})	2.6	9.3	3.95	4.19
TNEA (mG $Hz^{-1/2}$)	1	0.7	–	4.13

This study also established the test setup as shown in figure 9(*a*) to evaluate structure deformation due to the thermal change. The chip with the accelerometer was heated by the hot plate with temperature specified by the controller. Thermal deformation was characterized using the optical interferometer. The profiles in figure 9(*b*) were measured from the BB′ cross section of the accelerometer without Ni blocks as temperature ranges from 30 to 90 °C. The initial deflection of the proof mass is approximately 8 μm at room temperature. The measurement results in figure 9 depict that the bending curvatures of the MEMS structures with and without Ni electroplating were nearly the same at room temperature. It indicates that the residual stress of the Ni film did not cause the bending deformation of the suspended MEMS structure. As temperature increased from 30 to 90 °C, the radius of curvature of the proof mass was changed from 2.17 to 1.31 mm. In addition, figure 9(*c*) shows the measured CC′ cross-section profiles of the accelerometer with Ni blocks. As temperature increased from 30 to 90 °C, the radius of curvature of the proof mass was changed from 2.14 to 2.08 mm. As a result, the structure with Ni blocks has a smaller thermal deformation caused by the temperature variation. Such improvement attributes to the higher equivalent stiffness of the structure with selective electroplating Ni. Thus, the unwanted structure deformation due to temperature variation is significantly suppressed by electroplating Ni blocks. Finally, table 3 further summarizes the comparison of the proposed accelerometer with the existing 1-axis ones.

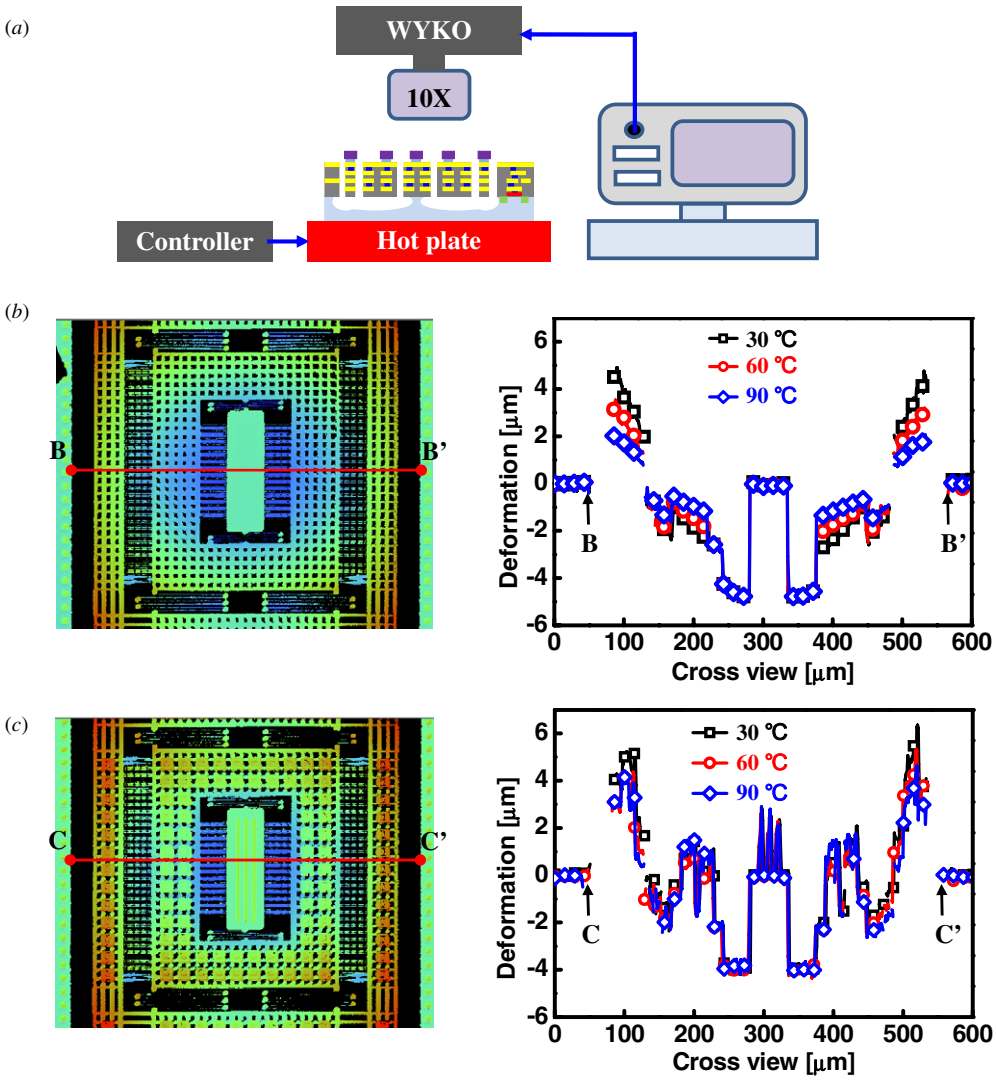


Figure 9. (*a*) Measurement setup to characterize the structure deformation of the accelerometer at different temperatures, the measured structure deformation of (*b*) the accelerometer without Ni and (*c*) the accelerometer with Ni.

5. Conclusions

In this study, a selective electroplating nickel on the CMOS-MEMS capacitive accelerometer has been proposed and successfully implemented based on the standard TSMC 0.35 μm 2P4M process. Measurements indicate that the sensitivity is improved 2.85-fold, noise is decreased near 1.7-fold, and the minimum detectable signal is improved from 1 to 0.2 G, after the Ni electroplating on the accelerometer. Furthermore, the stiffness of the suspended MEMS structure can be selectively increased, and thus the unwanted structure deformation caused by the temperature variation is significantly suppressed. The thickness uniformity may cause the performance deviation of the present devices. Moreover, the peel off of Ni blocks will not only cause the performance change but also lead to the problems of device movement and short circuit between the sensing electrodes. This study shows that the variation of the Ni thickness is 4.01 $\pm$ 0.22 μm under the same electroplating conditions. However, the thickness uniformity of electroplated Ni blocks can be further improved by the professional foundry. The device has no peel-off problem after fabrication. Nevertheless, the reliability test regarding the peel off of Ni blocks needs to be performed. In summary, this study presented an easy and low-temperature post-CMOS electroplating technology to improve the performance of the CMOS-MEMS devices. The applications of this approach can further extend to other CMOS-MEMS devices such as the magnetic sensor, resonator, etc.

Acknowledgments

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