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A pseudo 3D glass microprobe array: glass microprobe with embedded silicon for alignment and electrical interconnection during assembly

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Abstract
This study presents a process for the assembling of a pseudo 3D glass microprobe array. A glass microprobe with embedded silicon (ES) is batch fabricated by a glass reflow process. The silicon fixture and carrier for the assembly are also batch fabricated by silicon micromachining processes. First, the chips with a glass microprobe array are bonded by parylene-C to form the pseudo 3D glass microprobe array. The pseudo 3D microprobe array is then mounted on the silicon carrier. ES is employed for alignment during the assembly, and also acts as the electrical routing for signal recording. In application, the impedance of this glass microprobe is measured, and at 1 kHz it is 1.1 MΩ. Action potentials from rat brain cortex are also successfully recorded.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Neurons in the brain comprise a complex circuit. Information about how this circuit works is important for neural prostheses and neural disease detection/treatment [1]. The brain machine interface (BMI) system is an information bridge between neurons and the world. Microprobe arrays are key components of the BMI system. To date, microprobe arrays with different materials have been fabricated by microelectro-mechanical systems (MEMS) technology [2–10]. MEMS microprobes have the characteristics of well-defined electrode size and spacing, multiple electrodes on a single probe shaft and ease of integration with signal process circuits. Thus, the MEMS microprobe is considered a promising tool for neuroprostheses and brain circuit research. However, microprobe arrays implemented by MEMS technology are usually of a planar 2D in-plane structure. Such 2D in-plane microprobe arrays can only record neural signals from a 2D planar brain region [2–7], so that the recording area is restricted and the information received from the brain is limited. Thus, a 3D microprobe array structure would be preferable for neuroscience research and neural prostheses in order to improve both the recording density and range of the microprobe array.

There are various approaches for fabricating a 3D microelectrode array. An out-of-plane 3D microprobe array has been directly fabricated onto a silicon substrate [8–10], and planar-fabricated 2D polymer probes can be bent to form a 3D microprobe array [11, 12]. As reported in [13–19], in-plane 2D microprobe arrays have been fabricated individually and then manually assembled on a carrier to form a 3D microprobe array. The carrier was employed not only to support the 3D

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structure but also to transmit the neural signal to a back-end amplifier. In this regard, the probe length and the electrode number on each probe were not limited by the process, thus making it possible to achieve a higher density array. However, alignment and lead transfer are two important issues when implementing a 3D microprobe array, as the microprobe needs to transmit the electrical signal to a carrier perpendicular to the microprobe. Many techniques have been employed to implement 3D microprobe arrays, including nickel plating from the connection pad on the carrier to the microprobe chip [13], bending a thick gold beam onto the microprobe chip/carrier to connect the carrier/microprobe chip [14–17], and bonding an individual microprobe and flexible cable to form the electrical connection [18, 19].

Glass is a promising material for microprobe assembly. Unlike silicon, glass is a good insulator, eliminating parasitic capacitance crosstalk between electrodes [7]. Glass also has better biocompatibility than silicon [7, 20, 21]. As compared to a polymer microprobe, glass provides the microprobe with enough stiffness to insert it into the brain. This study employed the glass reflow technique to fabricate a glass microprobe array with embedded bulk silicon [7, 22]. Most importantly, an assembly technique has been demonstrated by realizing the glass microprobe array.

2. Fabrication and assembly processes

To demonstrate the assembly concept, microprobe has one electrode per shaft have been fabricated and assembled. The design concept of the assembling processes is illustrated in figure 1. As indicated in figure 1, the array consists of microprobes with either the same shaft length or different shaft lengths. Thus, the assembled microprobe array is named as the pseudo 3D array in this study. The glass microprobe with embedded low-resistance silicon was fabricated by the glass reflow process [7, 22]. This study further employed two assembly steps, namely 'stacking' and 'plug-in,' to implement the pseudo 3D glass microprobe array. In the 1st assembly step (stacking), the chips containing the glass microprobe array were stacked and bonded to form a pseudo 3D glass microprobe array. The alignment structures, such as the embedded silicon (ES) and the glass stick, as indicated in figure 1, were developed in this study so as to align the microprobe chips during this 1st step. For the 2nd assembly step (plug-in), the pseudo 3D glass microprobe array was further bonded to a silicon carrier. Meanwhile, the electrodes distributed on the microprobe array were re-routed to the wires patterned on the silicon carrier. The ES alignment structure in the 1st step was also employed as the electrical interconnection between the microprobe and the silicon carrier. Finally, it was easy to further integrate the application-specific integrated circuit (ASIC) chip on the silicon carrier for signal processing. A detailed description of the fabrication and assembly processes follows.

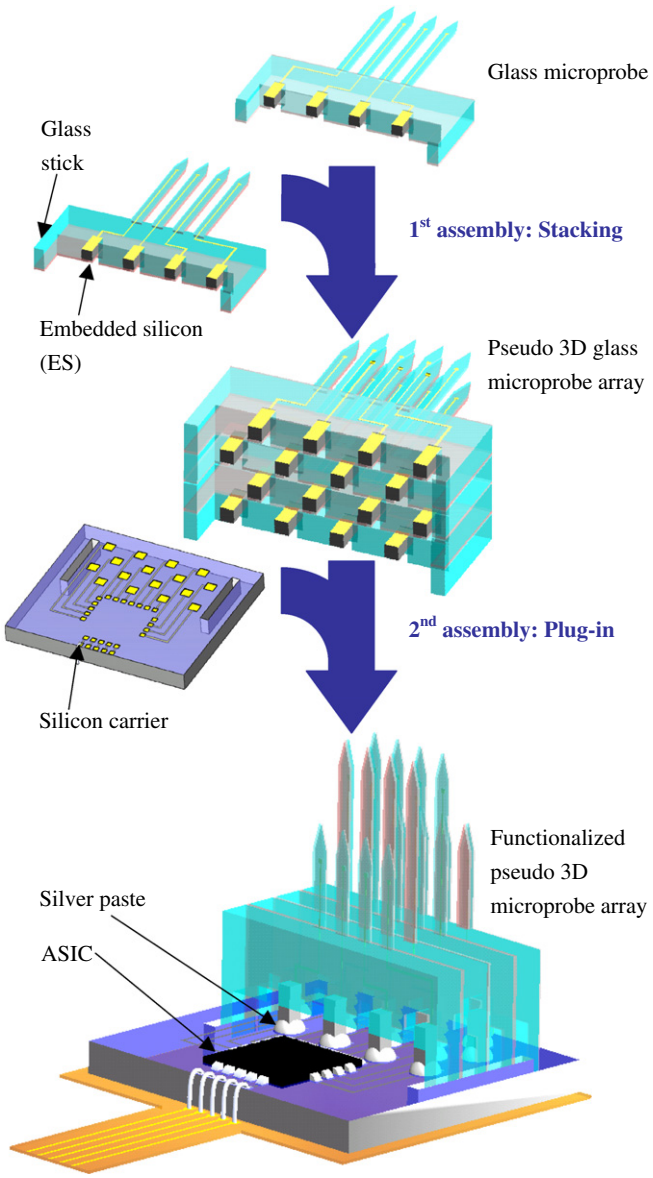

Figure 1. Design concept of a glass microprobe array with embedded silicon (ES) and the two assembling steps required to implement the pseudo 3D glass microprobe array.

2.1. Fabrication processes

Figure 2 shows the fabrication process steps at the AA′ cross section of the glass microprobe. As shown in figure 2(*a*), a thermal oxide on the low-resistance silicon wafer was patterned by the reactive ion etching process (RIE), and then the photoresist (PR) was coated and patterned. The PR was used as the etch mask for the 1st deep reactive ion etching process (DRIE) to define the microprobe base, as illustrated in figure 2(*b*), and it was removed by an H_2SO_4 solution ($H_2SO_4 : H_2O_2 = 3{:}1$). Silicon dioxide served as the 2nd etch mask for the 2nd DRIE to define the shape of the microprobe. Next, the silicon dioxide was removed by a buffered oxide etching solution (figure 2(*c*)). Pyrex 7740 glass was then bonded to the silicon wafer in a vacuum chamber by anodic bonding, and the bonded wafer was heated at 750 °C for 7 h in atmosphere to reflow the glass into the silicon mold. As shown in figure 2(*d*), a lapping process removed the excess glass and flattened the Si/glass surface. The metal wire (Ti/Au) was deposited by e-gun evaporation and followed by a

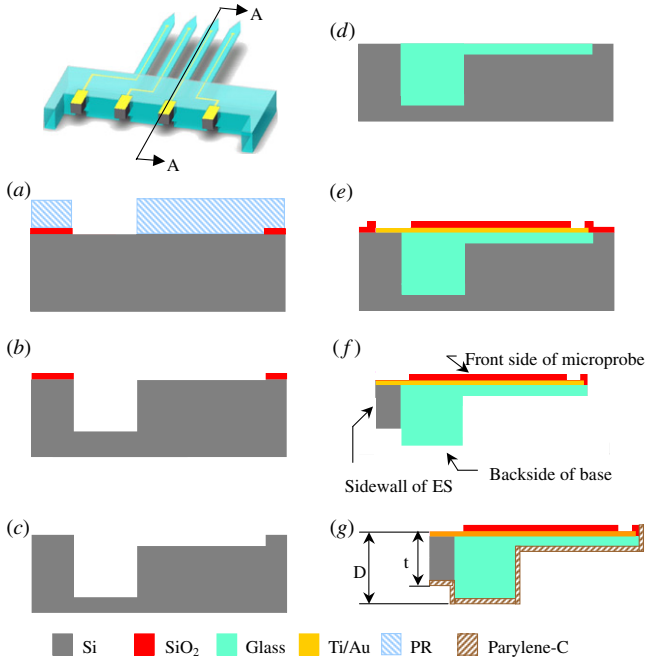

Figure 2. Fabrication process of glass microprobe with embedded silicon (ES) in AA's cross section: (*a*) the photoresist (PR) and patterned thermal oxide are the masks for the 1st DRIE and 2nd DRIE; (*b*) the 1st DRIE defines the shape of the microprobe base plate; (*c*) the 2nd DRIE defines the shape of the microprobe; (*d*) glass (Pyrex7740) is reflowed into the silicon mold and followed by a lapping process to remove excess glass; (*e*) the metal line (Ti/Au) and patterned by a lift-off process and followed by patterning the PECVD silicon dioxide; (*f*) the two-step DRIE process releases the microprobe and defines the thickness of ES; (*g*) parylene-C is patterned on the microprobe. The dimensions D (330 μm) and t (125 μm) in (*g*) are the thicknesses of ES and the microprobe base, respectively.

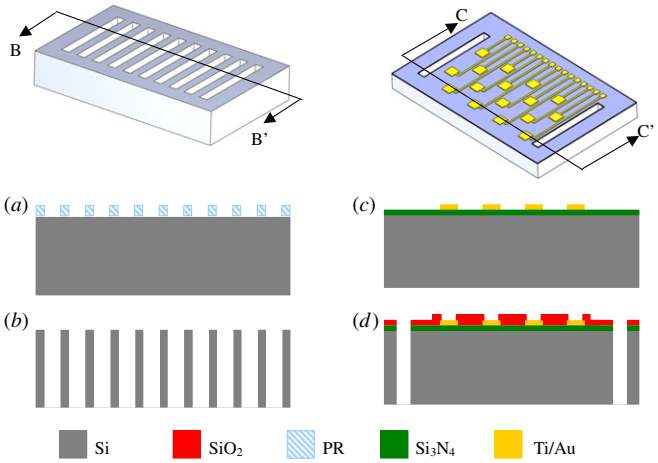

Figure 3. Fabrication processes of silicon fixture in the BB′ cross section: (*a*) photoresist pattern of the silicon trench, and (*b*) a through-wafer DRIE defines the alignment trench of the silicon fixture. Silicon carrier in the CC′ cross section (*c*) wafer first deposits silicon nitride as an insulation layer. A lift-off process defines the metal line and (*d*) the insulation silicon dioxide are patterned by a RIE process and followed by a DRIE process to define the alignment trench.

lift-off process. The silicon dioxide for insulation was deposited by plasma-enhanced chemical vapor deposition (PECVD) and then patterned by RIE to form the electrode and connection pad, as illustrated in figure 2(*e*). After that, the substrate was etched by another two-step DRIE, as shown in figure 2(*f*). The 1st DRIE defined the thickness of the ES and the 2nd DRIE released the whole structure. Parylene-C was deposited by CVD as the adhesive layer for the bonding of the microprobe chips [23]. After that, O_2 plasma was used to remove the parylene-C on the front side of the microprobe and the sidewall of the ES, as indicated in figure 2(*f*). During the O_2 plasma etching, the chip was mounted on a tilting stage so that both the front side of the microprobe and the sidewall of the ES were removed, as illustrated in figure 2(*g*). Thus, the glass microprobe array with embedded silicon was realized.

This study also established the micromachining processes, as illustrated in figure 3, to batch fabricate the components, such as the silicon fixture and silicon carrier, for the following assembly. Figures 3(*a*) and (*b*) show the fabrication of the silicon fixture at the BB′ cross section. The alignment trench array on the silicon fixture was precisely defined and batch fabricated by DRIE silicon etching. Figures 3(*c*) and (*d*) illustrate the fabrication of the silicon carrier at the CC′ cross section. An insulating silicon nitride was first deposited on the wafer. The metal wire layer was then prepared by the lift-off process to form the connection pad for the glass microprobe and the wire bond, as shown in figure 3(*c*). An insulating oxide was then deposited and patterned to open the metal pad, and DRIE was employed to define the alignment trenches on the silicon carrier, as illustrated in figure 3(*d*).

2.2. *Assembly processes*

The two-step assembly processes are illustrated in figure 4. During the 1st assembly, shown in figures 4(*a*) and (*b*), the silicon fixture fabricated in figures 3(*a*) and (*b*) was placed on the heating stage. A stereomicroscope was employed to monitor the assembly process. The chips containing the microprobe array were easily aligned to each other by inserting the ES into the corresponding alignment trenches, as indicated in figure 4(*a*). After applying a compression force and heating at 260 °C for 2 h, these microprobe chips were stacked and bonded together by parylene-C to form the pseudo 3D glass microprobe array, as illustrated in figure 4(*b*).

Figures 4(*c*)–(*e*) show the 2nd assembly process. The silicon carrier fabricated in figures 3(*c*) and (*d*) was placed on a heating stage, as shown in figure 4(*c*). After that, the Au pads on the silicon carrier were manually dispensed with silver paste using a commercial pneumatic dispensing workstation (EFD 2400) for the following bonding process. With the assistance of a micromanipulator, the glass sticks of the pseudo 3D microprobe array, prepared as shown in figures 4(*a*) and (*b*), were inserted into the trenches on the silicon carrier to ensure the alignment between the ES and the Au pads, as illustrated in figure 4(*d*). As indicated in the zoom-in illustration of figure 4(*e*), the alignment in both X and Y directions was

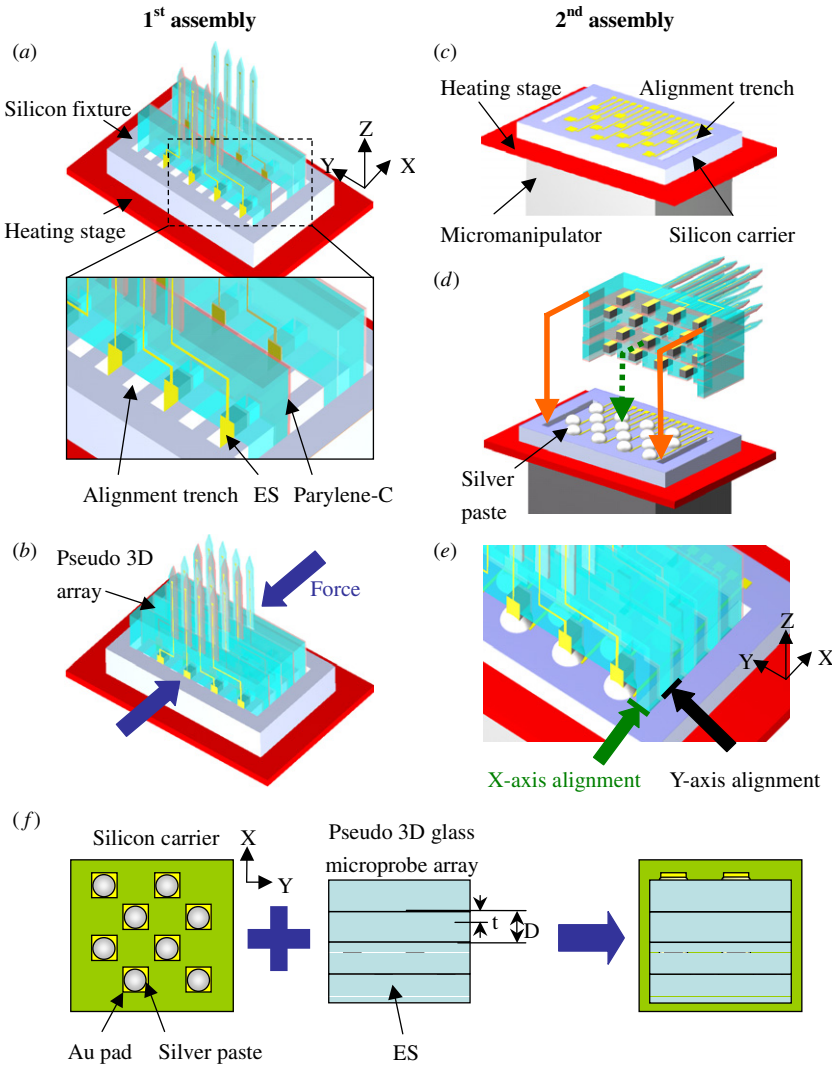

Figure 4. Detailed assembling processes and the concept of the 1st assembly process (*a*), (*b*): (*a*) insertion of ES into the alignment trench of the silicon fixture (the figure in the box is the enlarged view of the dashed box), and (*b*) the pseudo 3D microprobe array is assembled by applying a compression force and heat up to 260 °C for 2 h; and of the 2nd assembly process (*c*)–(*e*): (*c*) the silicon carrier is put on the heating stage and micromanipulator before assembly (*d*) silver paste is dispensed onto the silicon carrier. The pseudo 3D microprobe array is aligned to the silicon carrier by a glass stick (solid line). Thus, the ES can align to the corresponding Au pad (dash line), (*e*) *X*-axis alignment and *Y*-axis alignment are ensured by the alignment trench on the silicon carrier, and (*f*) the staggered design of the Au pads and ESs on the assembled array and the trimming process of ES reduce the probability of an electrical short between pads. *t* and *D* are the thicknesses of ES and the base plate, respectively.

assisted by the sidewalls of the trench. Thus, the ES on the pseudo 3D microprobe array was precisely in contact with the corresponding Au pad on the silicon carrier. Finally, the silver paste was cured at 130 °C for 20 min for bonding and the electrical connection.

As shown in figure 4(*d*), this study employed a staggered arrangement of Au pads and ESs to increase the yield of the 2nd assembly. The top illustrations in figure 4(*f*) show the staggered Au pads on the carrier and the staggered ESs on the bonded microprobe array. The staggered arrangement provided more spaces in the *X* direction, so that the tolerance during the 2nd assembly was significantly increased. Moreover, the ES thickness was trimmed to *t* by the DRIE process, as illustrated in figure 2(*f*). Thus, the planar dimensions of the ESs were smaller than those of the Au pad. This design prevented the short circuit resulting from the silver paste outflow during the 2nd assembly, as shown on the right of figure 4(*f*).

3. Results and discussion

This study has successfully demonstrated the fabrication and assembly by a pseudo 3D glass microprobe array. Moreover, the performance of the pseudo 3D glass microprobe array has also been characterized.

3.1. Fabrication results

The fabrication result in figure 5(*a*) shows the chip containing the glass microprobe with a 3 mm shaft length. Figure 5(*b*)

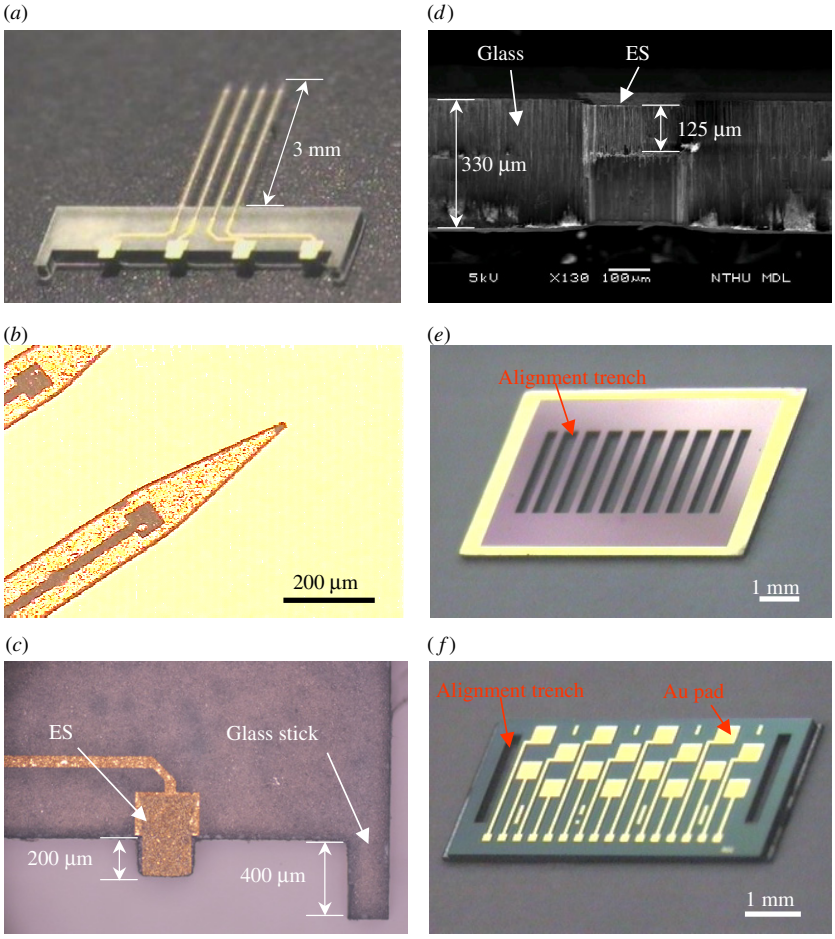

Figure 5. Fabrication results: (*a*) the glass microprobe with a 3 mm probe shaft, (*b*) the sharp tip of the glass microprobe, (*c*) the ES and glass stick arrangement, (*d*) thicknesses of glass substrate and ES, (*e*) silicon fixture and (*f*) silicon carrier.

shows the sharp tip fabricated by the glass reflow process. The close-up photo in figure 5(*c*) shows the glass stick and ES at the base plate of the microprobe. According to [10], the impedance between the two electrodes on the glass microprobe opened at 1 kHz; however, that on the silicon microprobe was about 20.2 MΩ at the same frequency. Thus, the ESs on the microprobes were electrically insulated from each other, and the neural signals recorded by the electrodes were transmitted to the ESs by the metal trace without channel crosstalk. The lengths of the glass stick and ES were 400 μm and 200 μm, respectively. Figure 5(*d*) shows the thickness of the glass substrate ($D = 330$ μm), and ES ($t = 125$ μm). Figure 5(*e*) shows a typical fabricated silicon fixture, and the alignment trenches for the insertion of ESs during the first assembly can be clearly observed. Figure 5(*f*) shows the silicon carrier with staggered Au pads for the connection of the microprobe array. In addition, the trenches for the alignment of the glass stick during the 2nd assembly can also be observed.

Figures 6(*a*)–(*d*) illustrate typical results of the pseudo 3D microprobe array (4 × 4) after the 1st assembly. Figure 6(*a*) shows the insertion of ES and the glass stick into the alignment trenches of the silicon fixture during the assembly. Figure 6(*b*) shows a typical 4 × 4 glass microprobe array after the 1st assembly process. The front-side view of the 4 × 4 microprobe array in figure 6(*c*) shows the stacking microprobes with shaft lengths of 1.8 mm and 3 mm. The distance between the probe shafts on different microprobe chips, which is defined by the thickness of the microprobe base plate, was 330 μm in this case. The back-side view of the 4 × 4 microprobe array in figure 6(*d*) shows the well alignment and the staggered arrangement of ESs. The arrangement of staggered ESs was matched with the position of the Au pads on the silicon carrier, as in figure 5(*f*). In short, the present assembly technique enabled the integration of chips containing microprobes of different shaft dimensions to form a pseudo 3D microprobe array for different applications, so long as those microprobes had the same ES arrangement.

Figures 6(*e*)–(*h*) show the 4 × 4 microprobe array bonded to the silicon carrier after the 2nd assembly process. The probe holder and the silicon carrier of this 4 × 4 microprobe array were 1.55 mm thick. The alignment between the ES and the Au pad was assisted by the trench and the glass stick, as indicated in figure 6(*e*). The electrical connection between the microprobe and the silicon carrier was provided by ES, silver paste and the Au pad, as indicated in figures 6(*f*) and (*g*). The assembled 4 × 4 glass microprobe array on the silicon carrier was then mounted on a flexible printed circuit board (PCB), as shown in figure 6(*h*). After wire bonding, a UV-curable polymer was used to encapsulate the 4 × 4 microprobe array

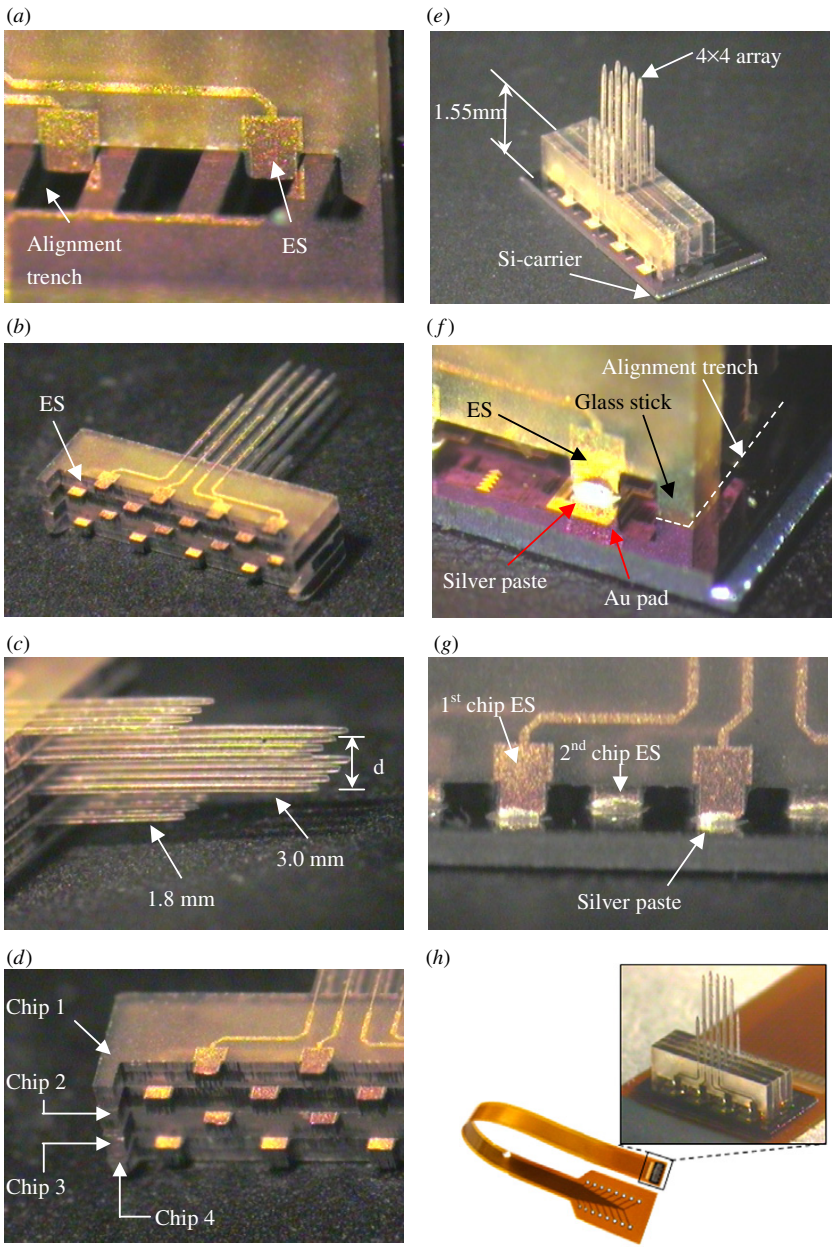

Figure 6. Assembling result of the 1st assembly (*a*)–(*d*): (*a*) ES and silicon fixture during 1st assembly, (*b*) typical 1st assembly result (4 × 4 microprobe array), (*c*) front-side view of the 4 × 4 microprobe array shows the integration microprobe with different shaft lengths. The distance between different microprobes (d) is defined by the base plate thickness, and (*d*) the back-side view of the 4 × 4 microprobe array illustrates the stacking of the microprobe arrays and the staggered arrangement of ES; and of the 2nd assembly (*e*)–(*h*): (*e*) 4 × 4 microprobe array and its silicon carrier. The thickness of the probe holder and the silicon carrier is 1.55 mm, (*f*) the glass stick and alignment trench on the silicon carrier ensure the alignment between the assembled array and the silicon carrier, (*g*) silver paste connects the ES and the silicon carrier with little outflow, and (*h*) a 4 × 4 microprobe array and Si carrier mounted on flexible PCB.

for electrical insulation, and the 4 × 4 microprobe array and the silicon carrier were then tightly bonded.

In summary, this study has demonstrated a novel ES design to enable the easy integration and electrical routing of pseudo 3D glass microprobe arrays. As compared with silicon, the glass had better biocompatibility [7, 20, 21]. Moreover, the glass microprobe array proposed in this study provided more flexibility on the microprobe shaft dimension and electrodes arrangement on shaft, as compared with the silicon microprobe array directly fabricated onto the silicon substrate [8–10]. In [8–10], the shaft length was limited by the wafer thickness or fabrication process. It was also challenging to implement shafts of different lengths on one chip. However, the drawback of the proposed glass microprobe was the requirement of an additional assembly process. On the other hand, as compared to the existing manual assembly methods for silicon microprobes in [13–17], the proposed assembly approach for the pseudo 3D glass microprobe in this study had different design aspects. In [16, 17], the base plate thickness of the microprobe needed to be precisely controlled in order to have a perfect fit during the assembly of the microprobe and carrier. In this study, the base plate thickness was influenced by various

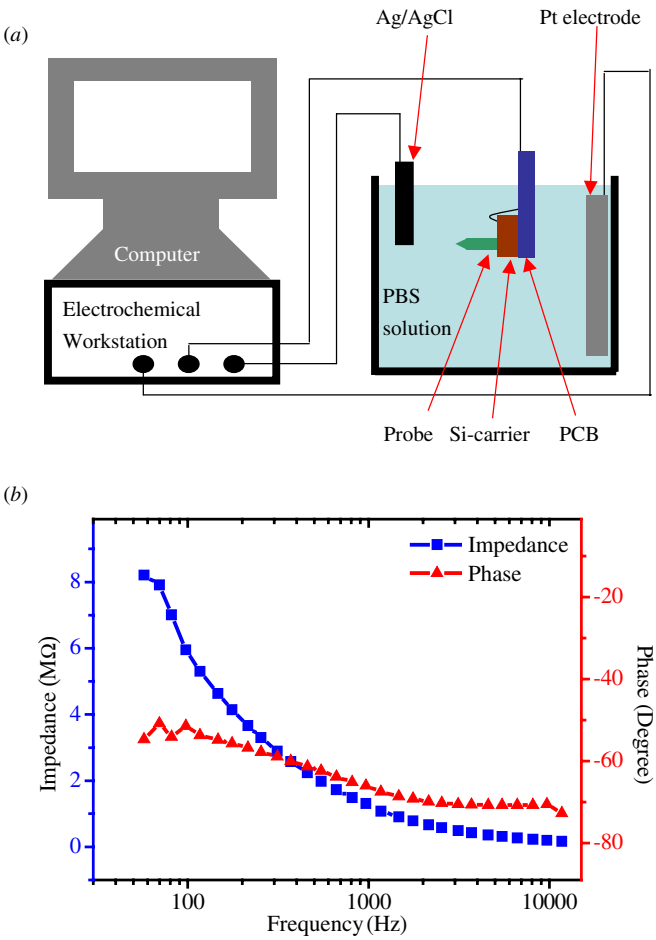

Figure 7. Impedance measurement. (*a*) The experiment setup; the microprobe (working electrode), the Ag/AgCl (reference electrode) and Pt electrode (counter electrode). (*b*) The measurement results.

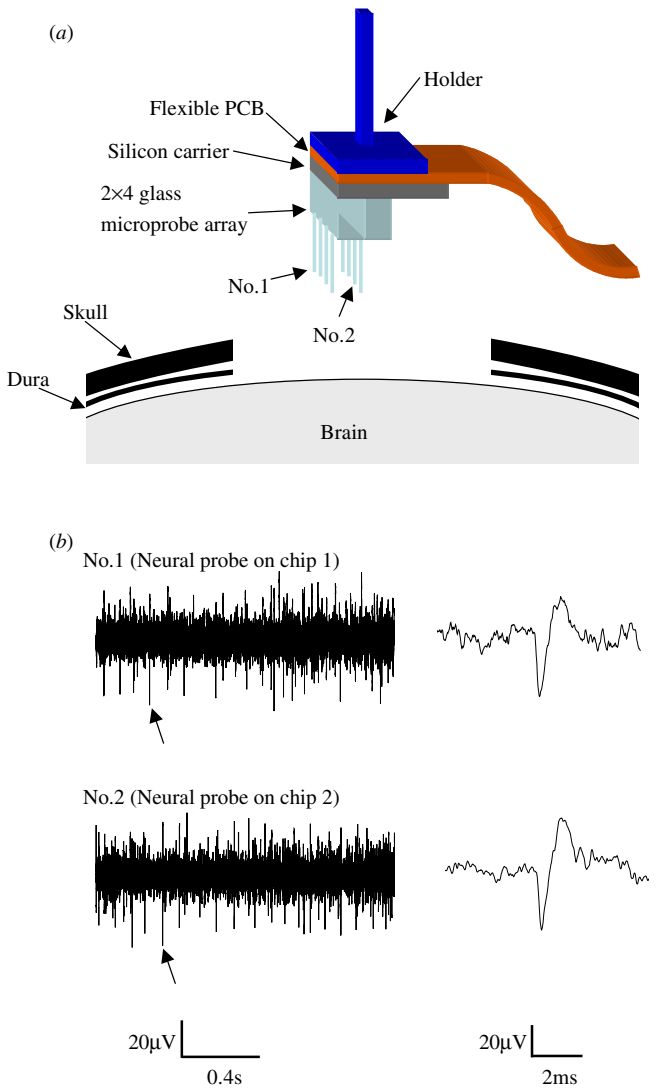

Figure 8. Action potentials recorded from rat M1 cortex: (*a*) packaged pseudo 3D microprobe array (2 × 4) is inserted into the brain tissue to record the spontaneous activity from the M1 cortex, and (*b*) the recorded signal from the neural probe on chip 1 and neural probe on chip 2 (locations as marked in (*a*)). The arrow points to two action potentials with a zoom in the image at the right of (*b*).

fabrication processes, such as the silicon mold patterned by DRIE (in figure 2(*c*)) and the lapping process (in figure 2(*d*)). Thus, it was difficult to precisely control base plate thickness. In this regard, the bulk ES was designed to allow for tolerance in the base plate thickness during assembly, as illustrated in figure 4(*f*). Furthermore, the array with 3D structure created an additional kill zone [24] if the microprobe shafts on different chips were not parallel to each other. In [13–15], the 3D array required special jigs and spacers to keep the shafts parallel on different microprobes. This study employed the 1st assembly process (stacking) to enable the microprobe shafts on different chips to be inherently parallel to each other.

3.2. Testing and results

The impedance of the pseudo 3D glass microprobe array was characterized to evaluate its performance. The 3-electrode setup in figure 7(*a*) was established to measure the impedance of the probe. The assembled glass microprobe array was immersed in the phosphate buffer saline (PBS, consisting of 149 mM NaCl, 2.6 mM KCl, 8 mM Na_2HPO_4 and 2 mM NaH_2PO_4, pH = 7.4) during measurement. The impedance and phase were measured by the Electrochemical Workstation (CH Instruments Inc.). The Ag/AgCl wire served as a reference electrode and a Pt electrode served as a counter electrode. A sinusoidal AC voltage with a peak-to-peak amplitude of 10 mV at a frequency range of 50 Hz to 10 kHz was applied to measure the impedance of the electrode on the assembled glass microprobe array. The measurement results are shown in figure 7(*b*). In this case, the impedance at the typical frequency of action potential (1 kHz) was about 1.1 MΩ. Moreover, in this study, the electrode was considered as a 'working electrode' as its impedance was lower than 5.0 MΩ. According to the measurement results, the assembly yield of the 3 × 4 microprobe array was almost 90%, and the impedance of the 'working electrodes' ranged from 1.1 MΩ to 4.2 MΩ.

Finally, the pseudo 3D microprobe array was also used to record neural activity in the motor cortex of a rat's brain (M1). The setup is shown in figure 8(*a*). The rat (male

Wistar rat, 250 g) was secured on a stereotaxic frame and anesthetized by Pento-barbital (50 mg cc^{-1}). A craniotomy was performed, and the dura was removed to expose the M1 cortex (AP: +2 mm, ML: +2.5 mm, to bregma). A packaged 2×4 microprobe array was fixed to the micromanipulator for precision positioning. The recorded signal was connected to a commercial differential amplifier (A-M systems, Model 1700) with a gain of 10 000. Figure 8(*b*) shows the neural activity simultaneously recorded by two electrodes on the 2×4 glass microprobe array (probe no1 on chip 1, and probe no 2 on chip 2, located as marked in figure 8(*a*)). In summary, this measurement successfully demonstrated the recording ability of the pseudo 3D glass microprobe array.

4. Conclusions

This study has demonstrated a glass reflow process to implement a glass microprobe with embedded silicon. The glass material inherently had better biocompatibility, and the electrodes on the glass microprobe also had lower crosstalk. The pseudo 3D microprobe array was further demonstrated after the bonding of the glass microprobe chips. The two-step assembly process to assemble the pseudo 3D glass microprobe array has been described. A novel ES structure was developed to ease alignment and electrical interconnection during assembly. The micromachined silicon fixture and carrier were also developed to ease the assembly process. Moreover, the staggered design of ESs on the microprobe chips as well as the Au pads on the silicon carrier allowed for greater tolerance in the 2nd assembly process. The trimmed ES prevented short circuiting between pads during the 2nd assembly. Thus, the assembly yield of the present approach was almost 90%. The impedance of the assembled glass microprobe array ranged from 1.1 MΩ to 4.2 MΩ at 1 kHz. The action potentials from the M1 cortex of a rat were successfully recorded by the pseudo 3D microprobe array.

Acknowledgments

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References

[1] Donoghue J P 2008 Bridging the brain to the world: a perspective on neural interface systems *Neuron* **60** 511–21

[2] Norlin P, Kindlundh M, Mouroux A, Yoshida K and Hofmann U G 2002 A 32-site neural recording probe fabricated by DRIE of SOI substrates *J. Micromech. Microeng.* **12** 414–9

[3] Moxon K A, Leiser S C, Gerhardt G A, Barbee K A and Chapin J K 2004 Ceramic-based multisite electrode arrays for chronic single-neuron recording *IEEE Trans. Biomed. Eng.* **51** 647–56

[4] Blanche T J, Spacek M A, Hetke J F and Swindale N V 2005 Polytrodes: high-density silicon electrode arrays for large-scale multiunit recording *J. Neurophysiol.* **93** 2987–3000

[5] Chan H Y, Aslant D M, Wang S H, Swain G M and Wise K D 2008 Fabrication and testing of a novel all-diamond neural probe for chemical detection and electrical sensing applications *Proc. of the 3rd IEEE Int. Conf. on Nano/Micro Engineered and Molecular Systems (Sanya, China)* pp 244–7

[6] Takeuchi S, Ziegler D, Yoshida Y, Mabuchi K and Suzuki T 2005 Parylene flexible neural probes integrated with microfluidic channels *Lab Chip* **5** 519–23

[7] Lin C W, Lee Y T, Chang C W, Hsu W L, Chang Y C and Fang W 2009 Novel glass microprobe arrays for neural recording *Biosens. Bioelectron.* **25** 475–81

[8] Bhandari R, Negi S, Rieth L, Normann R A and Solzbacher F 2009 A novel masking method for high aspect ratio penetrating microelectrode arrays *J. Micromech. Microeng.* **19** 035004

[9] Campbell P K, Jones K E, Huber R J, Horch K W and Normann R A 1991 A silicon-based, three-dimensional neural interface: manufacturing processes for an intracortical electrode array *IEEE Trans. Biomed. Eng.* **38** 758–68

[10] Takei K, Kawashima T, Kawano T, Takao H, Sawada K and Ishida M 2008 Integration of out-of-plane silicon dioxide microtubes, silicon microprobes and on-chip NMOSFETs by selective vapor-liquid-solid growth *J. Micromech. Microeng.* **18** 035033

[11] Rousche P J, Pellinen D S, Pivin D P Jr, Williams J C, Vetter R J and Kipke D R 2001 Flexible polyimide-based intracortical electrode arrays with bioactive capability *IEEE Trans. Biomed. Eng.* **48** 361–71

[12] Takeuchi S, Suzuki T, Mabuchi K and Fujita H 2004 3D flexible multichannel neural probe array *J. Micromech. Microeng.* **14** 104–7

[13] Hoogerwerf A C and Wise K D 1994 A three-dimensional microelectrode array for chronic neural recording *IEEE Trans. Biomed. Eng.* **41** 1136–46

[14] Bai Q, Wise K D and Anderson D J 2000 A high-yield microassembly structure for three-dimensional microelectrode arrays *IEEE Trans. Biomed. Eng.* **47** 281–89

[15] Yao Y, Gulari M N, Wiler J A and Wise K D 2007 A microassembled low-profile three-dimensional microelectrode array for neural prosthesis applications *J. Microelectromech. Syst.* **16** 977–88

[16] Aarts A A A, Neves H P, Puers R P and Van Hoof C 2008 An interconnect for out-of-plane assembled biomedical probe arrays *J. Micromech. Microeng.* **18** 064004

[17] Herwik S *et al* 2009 Fabrication technology for silicon-based microprobe arrays used in acute and sub-chronic neural recording *J. Micromech. Microeng.* **19** 074008

[18] Hetke J F, Williams J C, Pellinen D S, Vetter R J and Kipke D R 2003 3-D silicon probe array with hybrid polymer interconnect for chronic cortical recording *Conf. Proc. First Int. IEEE EMBS Conf. (Capri Island, Italy)* pp 181–4

[19] Du J, Roukes M L and Masmanidis S C 2009 Dual-side and three-dimensional microelectrode arrays fabricated from ultra-thin silicon substrates *J. Micromech. Microeng.* **19** 075008

[20] Bayliss S C, Buckberry L D, Fletcher I and Tobin M J 1999 The culture of neurons on silicon *Sensors Actuators* A **74** 139–42

[21] Christensen T B, Pedersen C M, Grondahl K G, Jensen T G, Sekulovic A, Bang D D and Wolff A 2007 PCR biocompatibility of lab-on-a-chip and MEMS materials *J. Micromech. Microeng.* **17** 1527–32

[22] Lin C W, Hsu C P, Yang H A, Wang W C and Fang W 2008 Implementation of silicon-on-glass MEMS devices with embedded through-wafer silicon vias using the glass reflow process for wafer-level packaging and 3D chip integration *J. Micromech. Microeng.* **18** 025018

[23] Kim H and Najafi K 2005 Characterization of low-temperature wafer bonding using thin-film parylene *J. Microelectromech. Syst.* **14** 1347–55

[24] Edell D J, Toi V V, McNeil V M and Clark L D 1992 Factors influencing the biocompatibility of insertable silicon microshafts in cerebral cortex *IEEE Trans. Biomed. Eng.* **39** 635–43